DIAMOND SYSTEMS CORPORATION

# Athena II User Manual

High Integration SBC with Ethernet and Data Acquisition

User Manual v1.03



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# Introduction

Athena II is an embedded single-board computer (SBC) in a custom PC/104 small form factor that integrates a complete embedded PC and data acquisition circuitry into a single board.

The single board Athena computer is a Pentium III class device with onboard central processing, memory and memory management devices and I/O management for specific functions. The board is larger than the PC-104 PCB format on three sides but uses the PC-104 mounting method and interface specification. The Athena II board includes the following additional features.

- Communicates externally over the ISA bus and I/O ports.
- Generates on-board RGB video for CRT display systems.
- Contains LVDS formatting to drive a flat panel
- Is powered from an externally regulated +5VDC supply.

Four models, shown in the following table, provide various speed, memory size and data acquisition options.

| ***Model*** | ***Processor Speed*** | ***RAM Size*** | ***Data Acquisistion*** |
|---|---|---|---|
| ATHM500-256A | 500 MHz | 256MB | Yes |
| ATHM500-256N | 500 MHz | 256MB | No |
| ATHM800-256A | 800 MHz | 256MB | Yes |
| ATHM800-256N | 800 MHz | 256MB | No |

The Athena II CPU uses the ISA bus, internally, to connect serial ports 1 through 4 and the data acquisition circuit to the processor. The ISA bus is brought out to an expansion connector to mate with add-on boards. Diamond Systems manufactures a wide variety of compatible PC/104 add-on boards for analog I/O, digital I/O, counter/timer functions, serial ports and power supplies.

## *Description and Features*

The Athena II board includes the following key system and data acquisition features.

### *Processor Section*

- 800MHz Mark CPU with integrated Northbridge, downclocked as needed to reduce power consumption.
- 256MB RAM, system memory.
- 100MHz memory bus.
- 512KB 16-bit wide integrated flash memory for BIOS and user programs.
- Advanced 2D/3D video graphics engine with integral MPEG-2 hardware acceleration.
- 33MHz PCI Bus.

### *I/O Section*

- 2 serial ports, 460k baud max.
- 2 serial ports, 115.2k baud max.
- 2 ports 16550-compatible.
- 2 ports 16850-compatible with 128-byte FIFOs. These ports provide RS-232 and automatic RS-485 half-duplex capability, and RS-485 termination.
- 4 USB 1.1 ports.
- IDE drive connectors; 44 pin notebook drive or solid-state flash disk connection.
- 10-/100 Base-T full-duplex PCI bus mastering Ethernet.
- CRT and 24-bit dual channel LVDS flat panel support.
- PS/2 keyboard and mouse ports.

- System status LEDs.
- Interface for amplified audio and additional LEDs.

### *Analog Input*

- 16 single-ended/8 differential inputs, 16-bit resolution.
- 100KHz maximum aggregate A/D sampling rate.
- Programmable input ranges/gains with maximum range of ±10V / 0-10V.
- Both bipolar and unipolar input ranges.
- 10 ppm/°C drift accuracy.
- Internal and external A/D triggering.
- 2048-byte sample FIFO for reliable high-speed sampling and scan operation.

### *Analog Output*

- 4 analog outputs, 12-bit resolution.
- ±10V and 0-10V output ranges available.
- ±5V and 0-5V output range (optional).

### *Digital I/O*

- 24 programmable digital I/O lines, 3.3V and 5V logic compatible, -0.5V to +5.5V tolerant.
- Enhanced output current capability: -8/+12mA max.

### *Counter/Timers*

- 1 24-bit counter/timer for A/D sampling rate control.
- 1 16-bit counter/timer for user counting and timing functions.
- Programmable gate and count enable.
- Internal and external clocking capability.

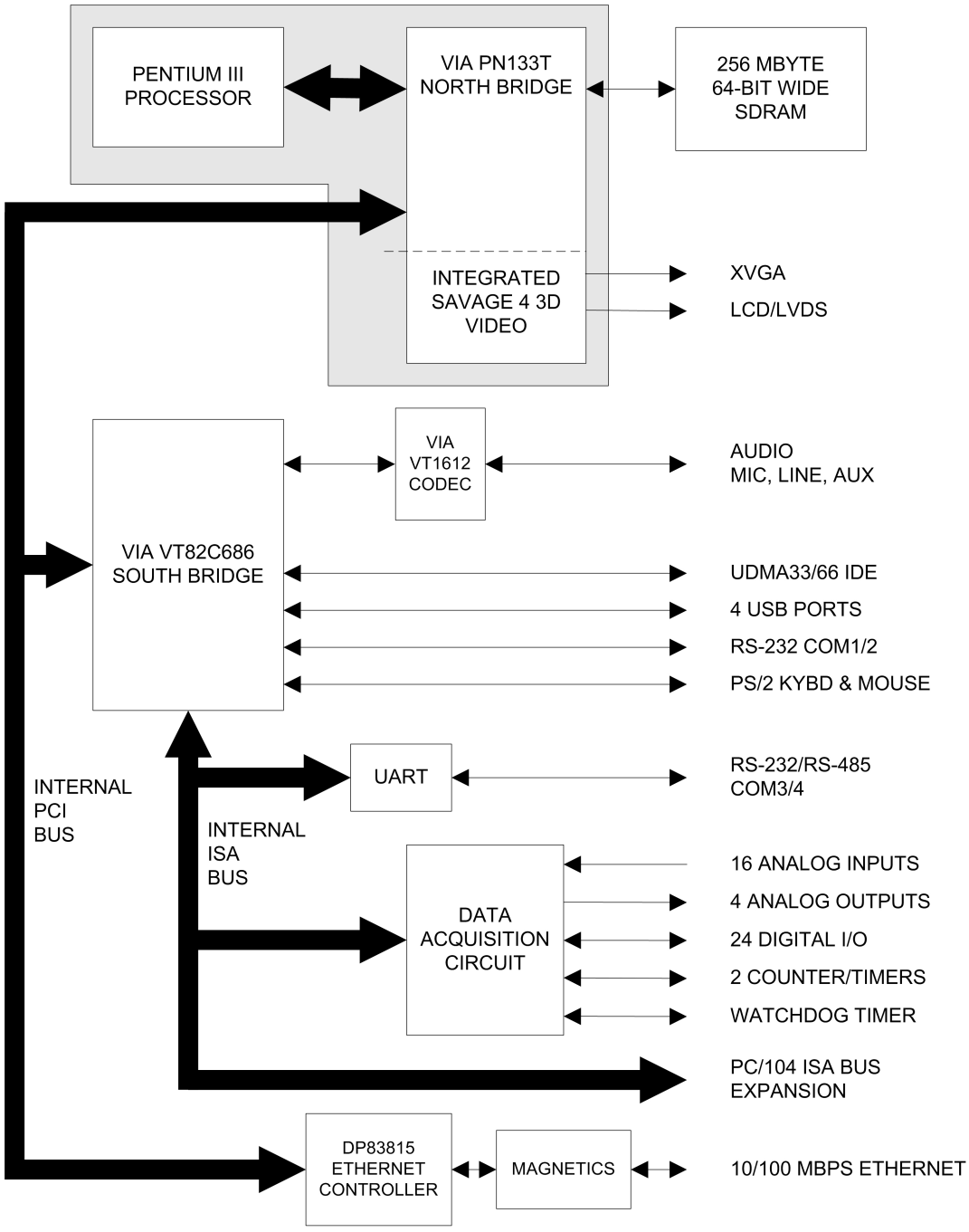
### *System Features*

- Plug and play BIOS with IDE auto detection, 32-bit IDE access, and LBA support.
- User-selectable COM1 or COM2 terminal mode.
- On-board lithium backup battery for real-time-clock and CMOS RAM.
- ATX power switching capability.
- Programmable watchdog timer.
- Power supply:  5VDC operation from the PC/104 bus or a power connector.
- Extended temperature range operation:  -40 to +85°C.

## *Block Diagram*

Figure 1 shows the Athena II functional blocks.

Figure 1: Athena II Block Diagram



## *Functional Overview*

This section describes the major Athena II subsystems.

### *Processor*

The board uses the VIA Mark integrated processor, with integrated Northbridge, up to the rated processor speed of 500/800MHz.

An appropriate heat sink is required, depending on the processor speed. The design supports a 5VDC fan with speed sensing. A connector is provided for this purpose.

### *Southbridge*

The VIA VT82C686 provides the ISA bus, audio, UDMA33/66 IDE, four USB 1.1 ports, two RS-232 ports and a PS/2 keyboard/mouse interface.

### *Memory*

The 64-bit wide 256MB SDRAM operates at 100MHz for all configurations. No expansion connector is provided for additional memory.

The board also includes flash memory for BIOS and user program storage. Flash memory is accessible through the on-board ISA bus.

### *Video Features*

Video circuitry is provided by the VIA Mark chipset.

### *Audio*

The design provides AC97 audio support derived from the Southbridge chip. The Via VT1612A CODEC provides audio processing.

Audio I/O includes,

- Stereo line in.
- Stereo line out.
- Mono mic in.
- Stereo internal line in.

The board includes audio power amplifier circuitry for stereo speaker output. The amplifier circuit is powered by +5VDC from the board. User DC control of volume is also provided, which overrides the software settings.

### *Ethernet*

The board supports 10-/100- Base-T Ethernet. Magnetics are included on the board so that a complete circuit is provided.

## *Data Acquisition*

The board provides the following data acquisition capabilities.

| ***Type of I/O*** | ***Characteristics*** |
|---|---|
| Analog Input | • 16 single-ended/8 differential inputs,16-bit resolution.<br>• 100KHz maximum aggregate A/D sampling rate.<br>• Programmable input ranges/gains: +/-10V, +/-5V, +/-2.5V, +/-1.25V, 0-10V, 0-5V, 0-2.5V.<br>• A/D FIFO for reliable high-speed sampling and scan operation. |
| Analog Output | • Four analog outputs, 12-bit resolution.<br>• ±10V and 0-10V output ranges.<br>• Indefinite short circuit protection on outputs. |
| Digital I/O | • 24 programmable digital I/O, 3.3V and 5V logic compatible. |
| Counter/Timers | • One 24-bit counter/timer for A/D sampling rate control.<br>• One 16-bit counter/timer for user counting and timing functions. |

On board $I^2C$ flash EEROM is provided for auto-calibration value storage.

## *Standard Peripherals*

The board provides the following standard system peripherals.

| ***Peripheral*** | ***Characteristics*** |
|---|---|
| Serial ports | Four serial ports |
| PS/2 ports | Keyboard and mouse |
| USB ports | Four USB 1.1 ports |
| IDE ports | One 44-pin connector for HDD or compact flashdisk socket |

Athena II contains four serial ports. Each port is capable of transmitting at speeds of up to 115.2Kbaud, and uses a dedicated RS-232 transceiver with ESD protection.

Ports COM1 and COM2 are built into the standard chipset, consisting of standard 16550-type UARTs with 16-byte FIFOs.

Ports COM3 and COM4 are derived from a dual UART chip, which includes 128-byte FIFOs. These ports may be operated at speeds up to 460Kbaud with the installation of high-speed drivers as a custom option. COM3 and COM4 can also be BIOS-selected for RS-232 or RS-485. Termination resistors can be jumper-enabled on these two ports.

Console redirection feature is incorporated. This feature enables keyboard input and character video output to be routed to one of the serial ports.

The board contains provision for mounting a solid state IDE flash disk module with capacities ranging from 32MB and greater. The module mounts onto the board using a 44-pin 2mm pitch header and a hold-down mounting hole with spacer and screws.

### *Bus Interfaces*

The PCI bus is generated by the VIA Mark processor module and is used internally for the Ethernet circuit. The PCI bus is not brought out to a PCI-104 expansion connector.

The Southbridge also provides the ISA bus, which is extended to the PC/-104 interface, ,providing the following I/O.

- Dual UART for 2 serial ports.
- Data acquisition circuit, including a watchdog timer, analog and digital I/O, and two counter/timers

### *Power Supply*

The power supply needs to supply an input voltage of +5VDC, ±5%, either from the PC/104 bus or from the on-board connectors.

The power supply includes ATX power switching and ACPI power management support.

**Note: The ATX power switch does not control the master +5V on the board.**

### *Battery Backup*

Athena II contains a backup battery for the real-time clock and BIOS settings. The battery is directly soldered to the board and provides a minimum 7 year backup lifetime at 25oC.

The on-board battery may be bypassed with a jumper or replaced with an external battery connected to an external battery connector.

### *Watchdog Timer*

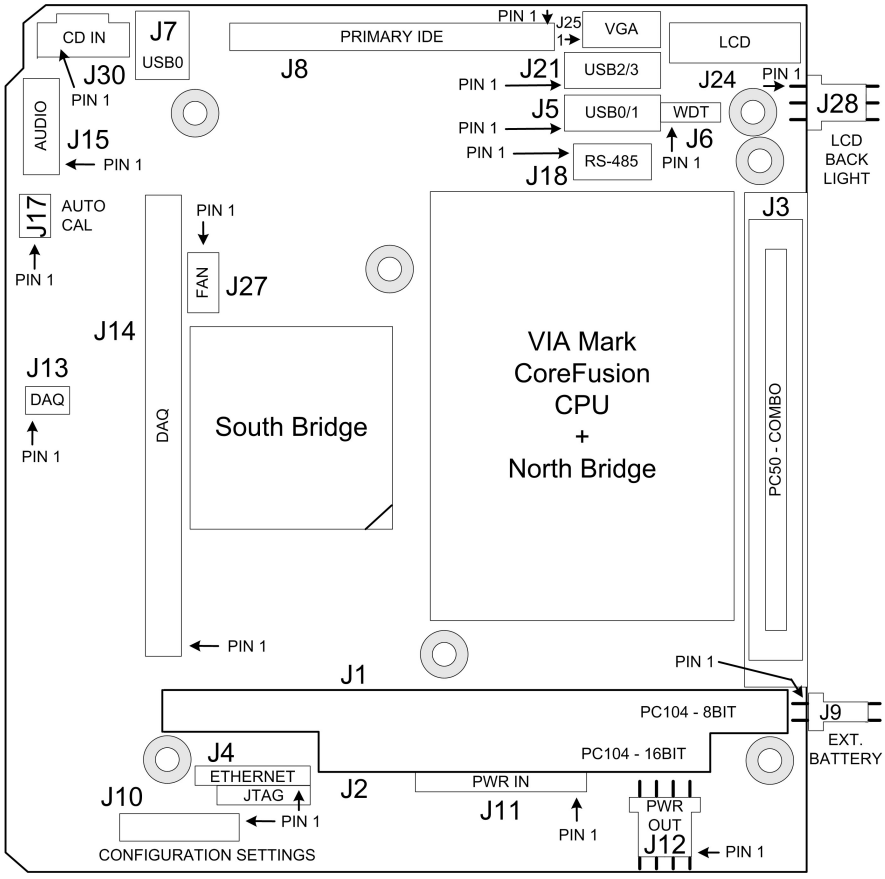
A watchdog timer (WDT) circuit consists of two cascaded programmable timers, which may be triggered in hardware or software.

## *Board Description*

### *Board Layout*

Figure 2 shows the Athena II board layout, including connectors, jumper blocks and mounting holes.

Figure 2: Athena II Board Layout



## *Connector Summary*

The following table lists the connectors on the Athena II board.

| *Connector* | *Description* |
|---|---|
| J1 | PC/104, ISA bus A,B |
| J2 | PC/104, ISA bus C,D |
| J3 | Main I/O (serial ports, PS/2 keyboard/mouse, parallel port, utility) |
| J4 | Ethernet |
| J5 | USB 0/1 |
| J6 | Watchdog/Failsafe Features |
| J7 | USB0 (mini-USB connector) |
| J8 | Primary IDE (44-pin, laptop) |
| J9 | External Battery |
| J11 | Input Power |
| J12 | External Auxiliary Power (output) |
| J14 | Data Acquisition I/O |
| J15 | Audio I/O |
| J17 | Auto-calibration Reference Voltage |
| J21 | USB 2/3 |
| J24 | LVDS LCD |
| J25 | VGA |
| J27 | CPU Fan |
| J28 | LCD Backlight Power |
| J30 | CD Input |

## *Jumper Summary*

The following table lists the jumpers on the Athena II board.

| *Jumper* | *Description* |
|---|---|
| J10 | System configuration (CPU features) |
| J13 | Data acquisition circuit configuration |
| J18 | RS-485 Mode Selection, COM 3/4 |

# Connectors

This section describes the on-board Athena II connectors.

> **Note: All cables mentioned in this chapter are included in Diamond Systems' cable kit C-ATH-KIT. Some cables are also available individually.**

## *PC/104 ISA Bus (J1, J2)*

Connectors J1 and J2 carry the ISA bus signals. The following diagram shows the PC/104 A and B pin layout for J1 and the C and D pin layout for J2.

***J1***

| | | | |
|---|---|---|---|
| IOCHCHK- | A1 | B1 | Ground |
| SD7 | A2 | B2 | RESETDRV |
| SD6 | A3 | B3 | +5V |
| SD5 | A4 | B4 | IRQ9 |
| SD4 | A5 | B5 | -5V |
| SD3 | A6 | B6 | DRQ2 |
| SD2 | A7 | B7 | -12V |
| SD1 | A8 | B8 | ENDXFR- |
| SD0 | A9 | B9 | +12V |
| IOCHRDY | A10 | B10 | Key |
| AEN | A11 | B11 | SMEMW- |
| SA19 | A12 | B12 | SMEMR- |
| SA18 | A13 | B13 | IOW- |
| SA17 | A14 | B14 | IOR- |
| SA16 | A15 | B15 | DACK3- |
| SA15 | A16 | B16 | DRQ3 |
| SA14 | A17 | B17 | DACK1- |
| SA13 | A18 | B18 | DRQ1 |
| SA12 | A19 | B19 | REFRESH- |
| SA11 | A20 | B20 | SYSCLK |
| SA10 | A21 | B21 | IRQ7 |
| SA9 | A22 | B22 | IRQ6 |
| SA8 | A23 | B23 | IRQ5 |
| SA7 | A24 | B24 | IRQ4 |
| SA6 | A25 | B25 | IRQ3 |
| SA5 | A26 | B26 | DACK2- |
| SA4 | A27 | B27 | TC |
| SA3 | A28 | B28 | BALE |
| SA2 | A29 | B29 | +5V |
| SA1 | A30 | B30 | OSC |
| SA0 | A31 | B31 | Ground |
| Ground | A32 | B32 | Ground |

***J2***

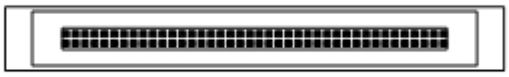
| | | | |
|---|---|---|---|
| Ground | C0 | D0 | Ground |
| SBHE- | C1 | D1 | MEMCS16-- |
| LA23 | C2 | D2 | IOCS16- |
| LA22 | C3 | D3 | IRQ10 |
| LA21 | C4 | D4 | IRQ11 |
| LA20 | C5 | D5 | IRQ12 |
| LA19 | C6 | D6 | IRQ15 |
| LA18 | C7 | D7 | IRQ14 |
| LA17 | C8 | D8 | DACK0- |
| MEMR- | C9 | D9 | DRQ0 |
| MEMW- | C10 | D10 | DACK5- |
| SD8 | C11 | D11 | DRQ5 |
| SD9 | C12 | D12 | DACK6- |
| SD10 | C13 | D13 | DRQ6 |
| SD11 | C14 | D14 | DACK7- |
| SD12 | C15 | D15 | DRQ7 |
| SD13 | C16 | D16 | +5 |
| SD14 | C17 | D17 | MASTER- |
| SD15 | C18 | D18 | Ground |
| Key | C19 | D19 | Ground |

### *Main I/O (J3)*

An 80-pin high-density connector, J3, is provided for access to the user I/O. The following functions are supported by this connector.

- Two serial ports
- Parallel port
- Watchdog timer I/O
- PS/2 keyboard
- PS/2 mouse
- IrDA port
- ATX Power switch
- Reset switch
- Power and HDD LEDs

Figure 3: J3 Main I/O Connector



| | | Cable A | Cable B | | |
|---|---|---|---|---|---|
| *COM1* | DCD1 | 1 | 1 | STB- | *LPT1* |
| | DSR1 | 2 | 2 | AFD- | |
| | RXD1 | 3 | 3 | PD0 | |
| | RTS1 | 4 | 4 | ERR- | |
| | TXD1 | 5 | 5 | PD1 | |
| | CTS1 | 6 | 6 | INIT- | |
| | DTR1 | 7 | 7 | PD2 | |
| | RI1 | 8 | 8 | SLIN- | |
| | GND | 9 | 9 | PD3 | |
| *COM2* | DCD2 | 10 | 10 | GND | |
| | DSR2 | 11 | 11 | PD4 | |
| | RXD2 | 12 | 12 | GND | |
| | RTS2 | 13 | 13 | PD5 | |
| | TXD2 | 14 | 14 | GND | |
| | CTS2 | 15 | 15 | PD6 | |
| | DTR2 | 16 | 16 | GND | |
| | RI2 | 17 | 17 | PD7 | |
| | GND | 18 | 18 | GND | |
| *COM3* | DCD3 | 19 | 19 | ACK- | |
| | DSR3 | 20 | 20 | GND | |
| | RXD3 | 21 | 21 | BUSY | |
| | RTS3 | 22 | 22 | GND | |
| | TXD3 | 23 | 23 | PE | |
| | CTS3 | 24 | 24 | GND | |
| | DTR3 | 25 | 25 | SLCT | |
| | RI3 | 26 | 26 | KB Clk | *KYBD* |
| | GND | 27 | 27 | KB/MS V- | |
| *COM4* | DCD4 | 28 | 28 | KB Data | |
| | DSR4 | 29 | 29 | KB/MS V+ | |
| | RXD4 | 30 | 30 | MS Clk | *Mouse* |
| | RTS4 | 31 | 31 | KB/MS V- | |
| | TXD4 | 32 | 32 | MS Data | |
| | CTS4 | 33 | 33 | KB/MS V+ | |
| | DTR4 | 34 | 34 | GND | *Utilities B* |
| | RI4 | 35 | 35 | Reset- | |
| | GND | 36 | 36 | ATX Power | |
| *Utilities A* | +5V Out | 37 | 37 | KB Lock | |
| | Speaker Out | 38 | 38 | IR RX | |
| | IDE Drive LED | 39 | 39 | IR TX | |
| | Power LED | 40 | 40 | +3VSB | |

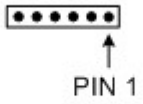
| *Signal Group* | *Signal* | *Description* |
|---|---|---|
| COM1-COM4 | - | The signals on these pins are RS-232 level signals and may be connected directly to RS-232 devices. The pinout of these signals is designed to allow a 9-pin male IDC connector to be crimped onto the corresponding ribbon cable wires to provide the correct pinout for a PC serial port connector (DTE). |
| LPT1 | - | The signals on these pins comprise a standard PC parallel port. The pinout of these signals is designed to allow a 25-pin female IDC connector to be crimped onto the corresponding ribbon cable wires to provide the correct pinout for a PC parallel port connector. |
| KYBD, Mouse | - | PS/2 signals for keyboard and mouse. (Pins 2 and 6 on the Mini-Din-6 PS/2 connectors are unused). |
| | KB Clk | Clock pin; connects to pin 5 of the PS/2 connector. |
| | KB/MS V- | Power pin; connects to pin 3 of the PS/2 connector. |
| | KB Data | Data pin; connects to pin 1 of the PS/2 connector. |
| | KB/MS V+ | Power pin; connects to pin 4 of the PS/2 connector. |
| Utilities A | +5V Out | Switched power pin that is turned on and off with the ATX power switch or with the +5V input. |
| | Speaker Out | Referenced to +5V Out. Connect a speaker between this pin and +5V Out. |
| | IDE Drive LED | Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out. |
| | Power LED | Referenced to +5V Out. Does not require a series resistor. Connect LED directly between this pin and +5V Out. |
| Utilities B | Reset- | Connection between this pin and Ground will generate a Reset condition. |
| | ATX Power | When ATX is enabled, a momentary contact between this pin and ground causes the CPU to turn on, and a contact of 4 seconds or longer will generate a power shutdown. ATX power control is enabled with a jumper on jumper block J10. |
| | KB Lock | When this pin is connected to Ground, the keyboard and mouse inputs are ignored. |
| | IR RX, IR TX | IrDA pins. Can be connected directly to an IrDA transceiver. |
| | +3VSB | Connected to +5V input power on J11. This pin is not switched by ATX control. This pin is provided for auxiliary use such as front panel lighting or other circuitry at the user's discretion. |

Connector J3 mates with Diamond Systems cable no. C-PRZ-01, which consists of a dual-ribbon-cable assembly with industry-standard connectors at the user end. The CPU mating connector includes integral latches for enhanced reliability. Each ribbon cable has 40 wires.

## *Ethernet (J4)*

Ethernet connectivity is provided by 1x6-pin connector J4. Connector J4 mates with Diamond Systems cable no. 698002, which provides a panel-mount RJ-45 jack for connection to standard CAT5 network cables.

Figure 4: J4 Ethernet Connector

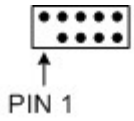



| | |
|---|---|
| 1 | Common |
| 2 | RX- |
| 3 | Common |
| 4 | RX+ |
| 5 | TX- |
| 6 | TX+ |

## *USB (J5, J21)*

Connectors J5 (USB 0/1) and J21 (USB 2/3) provide four USB 1.1 ports.

Figure 5: J5/J21 USB Connectors




| | | | |
|---|---|---|---|
| (J5-only) Key (pin cut) | 1 | 2 | Shield (J5-only) |
| GND | 3 | 4 | GND |
| USB1/3 D+ | 5 | 6 | USB0/2 D+ |
| USB1/3 D- | 7 | 8 | USB0/2 D- |
| USB1/3 VCC | 9 | 10 | USB0/2 VCC |

| *Signal* | *Definition* |
|---|---|
| VCC | +5VDC |
| D- | Data + |
| D+ | Data - |
| GND | Ground |

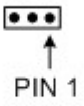
Connectors J5 and J21 mate with Diamond Systems cable no. 698012, which provides two standard USB type A jacks in a panel-mount housing.

**Note: USB0 (J7) shares the J5 USB circuitry. Do not connect USB devices to both USB0 and J5.**

## *Watchdog Timer (J6)*

Connector J6 is used for watchdog timer access..

Figure 6: J6 Watchdog Timer Access Connector




| | |
|---|---|
| 1 | GND |
| 2 | WDI |
| 3 | WDO |

| *Signal* | *Definition* |
|---|---|
| WDI | Watchdog Timer Input |
| WDO | Watchdog Timer Output |
| GND | 0V (ground) power return path. |

**Note: The watchdog timer circuit may be programmed either directly as described in this manual, or with the Diamond Systems Universal Driver software.**

## *USB0 (J7)*

Connector J7 (USB0) is a mini-USB connector that provides a single, quick and simple on-board USB connection for simple test and development without requiring an additional cable.

Figure 7: J7 USB0 Connector (end view)


| | |
|---|---|
| 1 | VCC |
| 2 | D- |
| 3 | D+ |
| 4 | (not used) |
| 5 | GND |

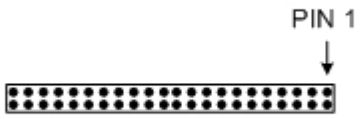
| *Signal* | *Definition* |
|---|---|
| VCC | +5VDC |
| D- | Data + |
| D+ | Data - |
| GND | Ground |

**Note: USB0 shares the J5 USB circuitry. Do not connect USB devices to both USB0 and J5.**

## *IDE (J8)*

Connector J8 is a 2x22-pin header used for an IDE connection. An associated mounting hole is provided to install a flash disk module.

Figure 8: J8 IDE Connector



| | | | |
|---|---|---|---|
| Reset - | 1 | 2 | Ground |
| D7 | 3 | 4 | D8 |
| D6 | 5 | 6 | D9 |
| D5 | 7 | 8 | D10 |
| D4 | 9 | 10 | D11 |
| D3 | 11 | 12 | D12 |
| D2 | 13 | 14 | D13 |
| D1 | 15 | 16 | D14 |
| D0 | 17 | 18 | D15 |
| Ground | 19 | 20 | Key (pin cut) |
| DRQ | 21 | 22 | Ground |
| IDEIOW- | 23 | 24 | Ground |
| IDEIOR- | 25 | 26 | Ground |
| IORDY | 27 | 28 | Ground |
| DACK- | 29 | 30 | Ground |
| IRQ14 | 31 | 32 | Pulled low for 16-bit operation |
| A1 | 33 | 34 | Not used |
| A0 | 35 | 36 | A2 |
| CS0- | 37 | 38 | CS1- |
| LED- | 39 | 40 | Ground |
| +5v | 41 | 42 | +5v |
| Ground | 43 | 44 | Not used |

Connector J8 mates with Diamond Systems cable no. 698004, and may be used to connect up to two IDE drives (hard disks, CD-ROMs, or flash disk modules). The 44-pin connector includes power and mates directly with notebook drives and flash disk modules. To use a standard format hard disk or CD-ROM drive with a 40-pin connector, an adapter PCB such as Diamond Systems ACC-IDEEXT is required.

**Note: Connector J8 supports only up to ATA-33 (UDMA-2). It does not support ATA-66 (UDMA-3 to 5) transfer modes.**

## *External Battery (J9)*

Connector J9 is used to connect an external battery for maintaining the Real-Time Clock and the CMOS settings (BIOS settings for various system configurations). The battery voltage for this input should be 3-3.6VDC. The current draw averages under 4µA at 3V.

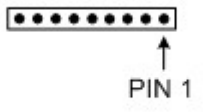
Figure 9: J9 External Battery Connector (end view)

| | |
|---|---|
| 1 | Battery input (+) |
| 2 | Ground |

## *Input Power (J11)*

Input power for Athena II may be supplied either from an external supply, through J11, or directly through the PC/104 bus power pins if a PC/104 power supply is used with the CPU.

Figure 10: J11 Input Power Connector




| | |
|---|---|
| 1 | +5V In |
| 2 | Ground |
| 3 | Key (pin cut) |
| 4 | +12V In |
| 5 | Ground |
| 6 | +5V In |
| 7 | -12V In |
| 8 | -5V In |
| 9 | ATX Control |

Input power for Athena may be supplied either through J11 from an external supply or directly through the PC/104 bus power pins if a PC/104 power supply is used with the CPU.

Athena requires only +5VDC input power to operate. All other required voltages are generated on board with miniature switching regulators. However since the PC/104 bus includes pins for ±5V and ±12V, these voltages may be supplied through J11 if needed. The +5V and +12V voltages are controlled by the ATX power manager switches, while -5V and -12V are routed directly to the corresponding pins on PC/104 bus and are not controlled by the ATX function.

Make sure that the power supply used has enough current capacity to drive your system. The Athena CPU requires up to 2A on the +5V line for the 500Mhz configuration (3.0A for the 800Mhz configuration.) If you have a disk drive or other modules connected, you need additional power. In particular, many disk drives need extra current during startup. If your system fails to boot properly, or if disk accesses do not work properly, the first thing to check is the power supply voltage level. Many boot-up problems are caused simply by insufficient voltage due to excess current draw on the +5V supply.

Multiple +5V and Ground pins are provided for extra current carrying capacity if needed. Each pin is rated at 3A max (15W). For the Athena CPU and panel I/O board 3A is sufficient, so +5V and Ground require only a single wire each. In this case the first 4 pins may be connected to a standard 4-pin miniature PC power connector if desired. Be advised that some voltage will be dropped in the wire depending on the wire gauge (AWG).

For a larger PC/104 stack the total power requirements should be calculated to determine whether additional wires are necessary.

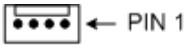
ATX control enables the +5V and +12V power to be switched on and off with an external momentary switch. A short press on the switch will turn on power, and holding the switch on for 4 seconds or longer will turn off power.

Diamond Systems' cable no. 698009 mates with J11. It provides 9 color-coded wires with stripped and tinned leads for connection to user-supplied power sources. When used, make sure the two red +5V wires are both connected to +5V.

## *External Auxiliary Power, Output (J12)*

Connector J12 provides switched power for use with external drives. If ATX is enabled, the power is switched ON and OFF with the ATX input switch. If ATX is not enabled, the power is switched ON and OFF in conjunction with the external power.

Figure 11: J12 Auxiliary Power Output Connector (end-on view)




| | |
|---|---|
| 1 | +5V (switched) |
| 2 | GND |
| 3 | GND |
| 4 | +12V (switched) |

| *Signal* | *Definition* |
|---|---|
| +5V | This is provided by the on-board power supply, derived from the input power. It is switched off when the board is powered down. |
| +12V | This is provided by the 12V input pin on the main power connector. It is switched off when the board is powered down. |
| GND | These are 0V ground references for the power output voltage rails, above. |

Diamond Systems cable no. 698006 mates with connector J12. This cable provides a standard full-size power connector for a hard drive or CD-ROM drive and a standard miniature power connector for a floppy drive.

### *Data Acquisition, Digital I/O (J14)*

Athena II includes a 50-pin header, J14, for all data acquisition I/O.

Figure 12: J14 Digital I/O Connector


| | | | |
|---|---|---|---|
| DIO A0 | 1 | 2 | DIO A1 |
| DIO A2 | 3 | 4 | DIO A3 |
| DIO A4 | 5 | 6 | DIO A5 |
| DIO A6 | 7 | 8 | DIO A7 |
| DIO B0 | 9 | 10 | DIO B1 |
| DIO B2 | 11 | 12 | DIO B3 |
| DIO B4 | 13 | 14 | DIO B5 |
| DIO B6 | 15 | 16 | DIO B7 |
| DIO C0 | 17 | 18 | DIO C1 |
| DIO C2 | 19 | 20 | DIO C3 |
| DIO C4/GATE0 | 21 | 22 | DIO C5/GATE1 |
| DIO C6/CLK1 | 23 | 24 | DIO C7/OUT0 |
| EXTTRIG | 25 | 26 | TOUT1 |
| +5V out | 27 | 28 | DGND |
| VOUT0 | 29 | 30 | VOUT1 |
| VOUT2 | 31 | 32 | VOUT3 |
| AGND(Vout) | 33 | 34 | AGND(Vin) |
| VIN0 | 35 | 36 | VIN8 |
| VIN1 | 37 | 38 | VIN9 |
| VIN2 | 39 | 40 | VIN10 |
| VIN3 | 41 | 42 | VIN11 |
| VIN4 | 43 | 44 | VIN12 |
| VIN5 | 45 | 46 | VIN13 |
| VIN6 | 47 | 48 | VIN14 |
| VIN7 | 49 | 50 | VIN15 |

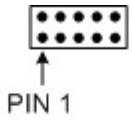
| *Signal* | *Definition* |
|---|---|
| DIO A7-A0 | Digital I/O port A; programmable direction. |
| DIO B7-B0 | Digital I/O port B; programmable direction. |
| DIO C7-C0 | Digital I/O port C; programmable direction. C7-C4 may be configured for counter/timer signals. |
| EXTTRIG | External A/D trigger input. |
| TOUT1 | Counter/Timer 1 output. |
| Vin 7/7+ ~ Vin 0/0+ | Analog input channels 7 – 0 in single-ended mode. High side of input channels 7 – 0 in differential mode. |
| Vin 15/7- ~ Vin 8/0- | Analog input channels 15 – 8 in both single-ended mode. Low side of input channels 7 – 0 in differential mode. |
| VOUT0-3 | Analog output channels 0 – 3. |
| +5V out | Connected to switched +5V supply (Output only! Do not connect to external supply). |
| DGND | Digital ground (0V - reference); used for digital circuitry only. |
| AGND | Analog ground; used for analog circuitry only. Vout pin is for analog outputs, Vin pin is for analog inputs. |

Diamond Systems cable no. C-50-18 provides a standard 50-pin connector at each end and mates with this header.

## *Speaker (J15)*

Connector J15 is a 2x5-pin header used to connect speakers.

Figure 13: J15 Speaker Connector




| | | | |
|---|---|---|---|
| Left headphone, line out | 1 | 2 | Right headphone, line out |
| Audio ground | 3 | 4 | Line input, left |
| Line input, right | 5 | 6 | Audio ground |
| Microphone input | 7 | 8 | Power reference for microphone |
| Key (pin cut) | 9 | 10 | Audio ground |

The volume control is capable of 32 discrete levels, ranging from a 20dB maximum gain to -85dB (Muted). The main volume control is the “MID” line, which may be tied to the center tap of a potentiometer with “HIGH” on one side and “LOW” on the other to give a full range of power control.

- Shorting “MID” to “LOW” mutes the speaker audio.

- Shorting “MID” to “HIGH” provides maximum gain.
- Default (no connection) provides 10dB of gain.

The maximum output power is specified to provide up to two Watts into a 4-Ohm speaker load. Note that this output power is drawn from the on-board 5V supply.

The speakers are driven using a Bridged-Tied Load (BTL) amplifier configuration. This is a differential speaker connection. As such, each speaker should be wired directly to the appropriate pair of connections for that speaker.

- Do not connect the speaker low sides (-) to ground
- Do not short the speaker low connections together.

## *Auto-Calibration Reference Voltage (J17)*

Connector J17 is a two-pin header used for auto-calibration.

| | |
|---|---|
| 1 | GND |
| 2 | AutoCal Reference Value |

The Diamond Systems AutoCal routines read the exact voltage calibration values from the AutoCal-Flash. There are four analog values that need to be measured and stored in the AutoCal flash during manufacturing test. Those values are produced from a very stable power source.

The values stored to AutoCal flash can be measured at header J17, where pin 1 is ground and pin 2 is one of the positive values shown in the following table, depending on the selection of the Cal-Mux. The table gives the approximate values of the four AutoCal values.

| *Cal-Mux* | *Value* |
|---|---|
| 0 | 5.5mV |
| 1 | 1.2V |
| 2 | 2.48V |
| 3 | 4.96V |

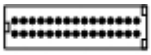
**Note: Disconnect the measurement cables after measuring the voltages and before initiating the actual auto-calibration.**

## *LCD Panel, LVDS Interface (J24)*

Connector J24 provides access to the internal LVDS LCD display drivers. Note that the LCD also requires the backlight to be connected (J28, below) to function correctly.

**Note: Connector J24 is not installed in the standard Athena II configuration.**

Figure 14: J24 LCD Panel Connector



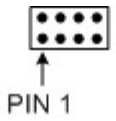
| | | | |
|---|---|---|---|
| Ground | 1 | 2 | Ground |
| LCD1 clock- | 3 | 4 | LCD2 clock- |
| LCD1 clock+ | 5 | 6 | LCD2 clock+ |
| Ground | 7 | 8 | Ground |
| LCD1 data 0- | 9 | 10 | LCD2 data 0- |
| LCD1 data 0+ | 11 | 12 | LCD2 data 0+ |
| Ground | 13 | 14 | Ground |
| LCD1 data 2- | 15 | 16 | LCD2 data 1- |
| LCD1 data 2+ | 17 | 18 | LCD2 data 1+ |
| Ground | 19 | 20 | Ground |
| LCD1 data 1- | 21 | 22 | LCD2 clock- |
| LCD1 data 1+ | 23 | 24 | LCD2 clock+ |
| Ground | 25 | 26 | Ground |
| VDD (LCD display) | 27 | 28 | VDD (LCD display) |
| VDD (LCD display) | 29 | 30 | VDD (LCD display) |

| ***Signal*** | ***Definition*** |
|---|---|
| LCD1 Data 0-2 +/- | Primary Data Channel, bits 0-2 (LVDS Differential signaling) |
| LCD1 Clock +/- | Primary Data Channel, Clock (LVDS Differential signaling) |
| LCD2 Data 0-2 +/- | Secondary Data Channel, bits 0-2 (LVDS Differential signaling) |
| LCD2 Clock +/- | Secondary Data Channel, Clock (LVDS Differential signaling) |
| VDD | +3.3V Switched Power Supply for LCD display (only powered up when LCD display is active) |
| Ground | Power Ground, 0V |

## *VGA (J25)*

Connector J25 is a 2x4-pin header for connecting a VGA monitor.

Figure 15: J25 VGA Connector




| | | | |
|---|---|---|---|
| Green | 1 | 2 | Red |
| Blue | 3 | 4 | Ground |
| HSYNC | 5 | 6 | DDC data |
| VSYNC | 7 | 8 | DDC clock |

| *Signal* | *Definition* |
|---|---|
| Ground | Ground return |
| Red | RED signal (positive, 0.7Vpp into 75 Ohm load) |
| Green | GREEN signal (positive, 0.7Vpp into 75 Ohm load) |
| Blue | BLUE signal (positive, 0.7Vpp into 75 Ohm load) |
| DDC clock/data | Digital serial I/O signals used for monitor detection (DDC1 specification) |
| HSYNC | Horizontal sync |
| VSYNC | Vertical sync |

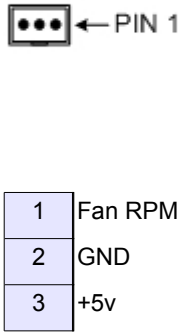
**Note: While the DDC serial detection pins are present, a 5V power supply is not provided (the old "Monitor ID" pins are also not used).**

Diamond Systems Cable Assembly 698024 provides a female DB15 connection to interface with a standard RGB monitor.

## *CPU Fan (J27)*

Connector J27 is used to connect to the CPU fan.

Figure 16: J27 CPU Fan Connector

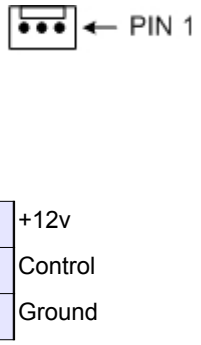



| *Signal* | *Definition* |
|---|---|
| Fan RPM | TTL signal input that pulses with each revolution of the fan. |
| +5 | Power Supply for optional CPU Fan, if necessary. |
| GND | Ground |

## *LCD Backlight (J28)*

Connector J28 provides the backlight power and control for the optional LCD panel. See the description for connector J24, above, for details on the LCD data interface.

Figure 17: J28 LCD Backlight Connector (end view)




| *Signal* | *Definition* |
|---|---|
| +12V | Power supply for LCD Backlight assembly |
| Control | Output signal (from Athena II) to allow power-down of backlight |
| Ground | Ground for LCD Backlight assembly |

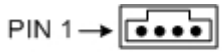
Connector J28 provides the backlight power and control for the optional LCD panel. See the description for connector J24, above, for details on the LCD data interface.

> **Note: The +12V supply will be removed when the system is powered down. The control signal is used to allow the system to power-down the backlight when the system enables monitor-power-down during its power management control. A 12V power supply must be provided either on the J11 input power connector, or on the 12V pin on the PC/104 connector for the LCD backlight to operated. This voltage is not generated internally.**

## *CD Input (J30)*

The J30 connector is for a PC-standard CD input cable, which provides the CD Audio Input to the AC97 Sound circuitry.

Figure 18: J30 CD Input Connector




| | |
|---|---|
| 1 | Left CD input |
| 2 | Left ground |
| 3 | Right ground |
| 4 | Right CD input |

The connector is an industry-standard CD-IN connector, which is common in most desktop Personal Computers. Note that the left and right grounds are decoupled but are also tied together on-board. This input is intended for CD-input only; i.e., no amplified or microphone inputs.

# Board Configuration

The Athena II board has the following jumper-selectable configuration options.

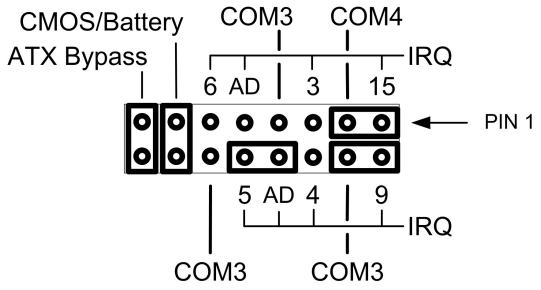
**Note: Connector J10 is not installed on the standard Athena II board.**

| *Jumper Block* | *Configuration Functions* |
|---|---|
| J10 | System configuration jumper block. |
| J13 | Data acquisition circuit configuration jumper block. |
| J18 | RS-485 mode selection jumper block. |

## *System Configuration (J10)*

Jumper block J10 is used to configure IRQ levels, ATX power control and CMOS RAM.

Figure 19: J10 Jumper Block with Default Settings




| *J10* | |
|---|---|
| ***Pin Label*** | ***Function*** |
| BAT | Battery connected:<br>in - battery connected<br>(CMOS RAM settings preserved)<br>out - battery not connected<br>(CMOS RAM settings erased) |
| ATX | ATX power control<br>in - ATX-like power control<br>out - standard (powers up immediately) |
| 3 | IRQ 3; selectable for COM3, COM4 |
| 4 | IRQ 4; selectable for COM3, ADC |
| 5 | IRQ 5; selectable for COM3, ADC |
| 6 | IRQ 6; selectable for COM3, ADC |
| 9 | IRQ 9; selectable for COM3 |
| 15 | IRQ 15; selectable for COM4 |

## *Serial Port and A/D IRQ Settings*

COM3, COM4 and A/D IRQ settings can be configured as shown in the following table.

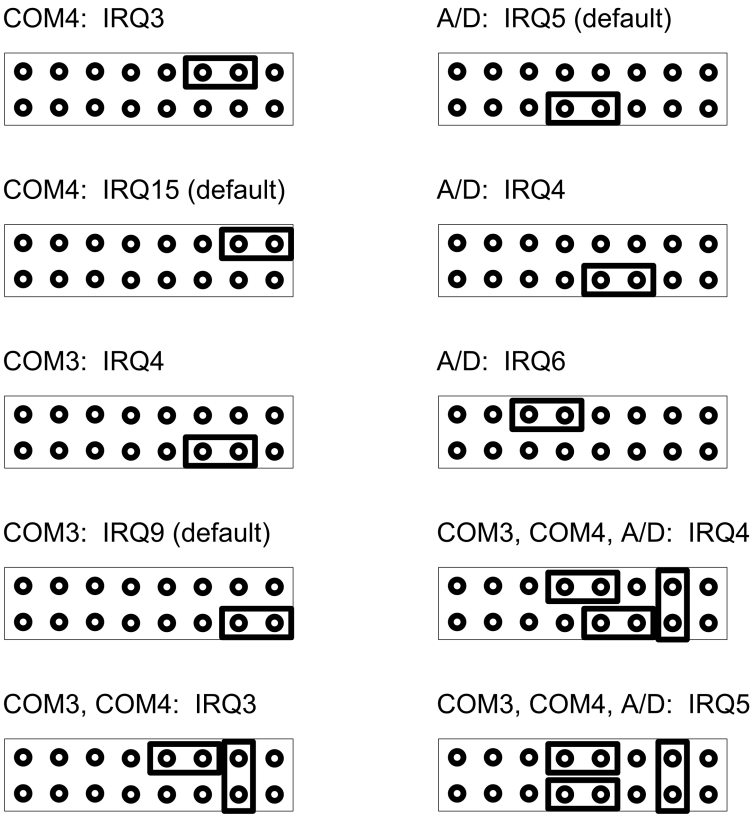
| *Device* | *IRQ3* | *IRQ4* | *IRQ5* | *IRQ6* | *IRQ9* | *IRQ15* |
|---|---|---|---|---|---|---|
| COM3 | X | X | X | X | X (default) | - |
| COM4 | X | - | - | - | - | X (default) |
| A/D | - | X | X (default) | X | - | - |

**Note: IRQ4 can only be used for A/D if it is not already used for COM3.**

It is possible to set up all three circuits to share either IRQ4 or IRQ5. However, only one device can use the shared IRQ at a time; the ability for all three devices to run simultaneously is not supported.

Configure the IRQ options as shown in the following jumper settings.

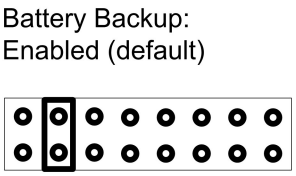
Figure 20: IRQ Configuration Options



### *Erasing CMOS RAM Settings*

With the jumper in place (enabled, as shown in Figure 21) the CPU powers up with the default BIOS settings.

Figure 21: CMOS RAM Jumper Settings




Follow these steps to clear the CMOS RAM.

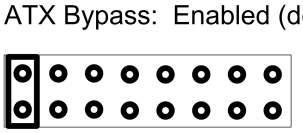
1. Power-down the CPU.
2. Remove the BAT jumper.
3. Wait a few seconds.
4. Insert the BAT jumper.
5. Power-up the CPU.

**Note: Before erasing CMOS RAM, write down any custom BIOS settings.**

### *ATX Power Control Settings*

The ATX power control is set using the J10 ATX jumper, shown in Figure 22.

Figure 22: ATX Power Control Jumper Setting




If the ATX jumper is out, ATX works normally, and an external, momentary switch may be used to turn power ON and OFF. A quick contact turns the power ON, and a long contact (greater than four seconds) turns the power OFF.

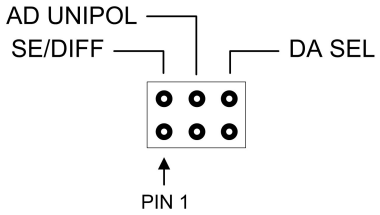
If the ATX jumper is in, the ATX function is bypassed and the system powers up as soon as power is connected. This is the default setting, as shown in Figure 22.

If the ATX jumper is removed, the battery-backup for CMOS does not function when power is removed.

## *DAC Configuration (J13)*

Jumper block J13 is used to configure the A/D and D/A circuits.

Figure 23: J13 Jumper Block




| *Jumper Label* | *Configuration Function* |
|---|---|
| SE/DIFF | A/D single-ended/differential selection. |
| AD UNIPOL | A/D unipolar/bipolar selection. |
| DA SEL | D/A unipolar/bipolar selection. |

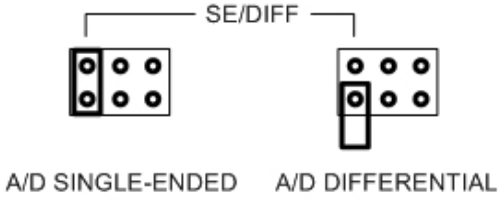
### *Single-ended/Differential Input Settings*

Athena II can accept both single-ended and differential inputs. A single-ended input uses two wires: input and ground. The measured input voltage is the difference between these two wires. A differential input uses three wires: input(+), input(–) and ground. The measured input voltage is the difference between the (+) and (–) inputs.

Differential inputs are frequently used either when the grounds of the input device and the measurement device (Athena II) are at different voltages, or when a low-level signal is being measured that has its own ground wire. A differential input also has higher noise immunity than a single-ended input because most noise affects both (+) and (–) input wires equally, so the noise is canceled out in the measurement. The disadvantage of differential inputs is that only half as many are available because two input pins are required to produce a single differential input.

Athena II can be configured for either 16 single-ended inputs, or eight differential inputs, as shown below. The default setting is single-ended mode.

Figure 24: A/D Single-ended/Differential Selection



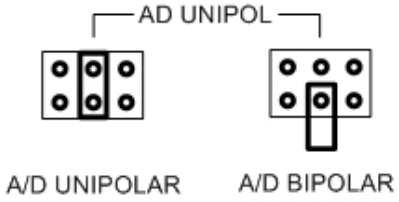

If you have a combination of single-ended and differential input signals, select differential mode. Then, to measure the single-ended signals, connect the signal to the plus (+) input and connect analog ground to the minus (–) input.

> **WARNING: The maximum range of voltages that can be applied to an analog input on Athena II without damage is ±35V. If you connect the analog inputs on Athena to a circuit whose ground potential plus maximum signal voltage exceeds ±35V, the analog input circuit may be damaged. Check the ground difference between the input source and Athena II before connecting analog input signals.**

### *Unipolar/Bipolar Input Settings*

The analog inputs can be configured for either unipolar (positive input voltages only), or bipolar (both positive and negative input voltages). For unipolar inputs, install a jumper as shown below. For bipolar inputs, omit the jumper. The default configuration is bipolar mode (jumper out).

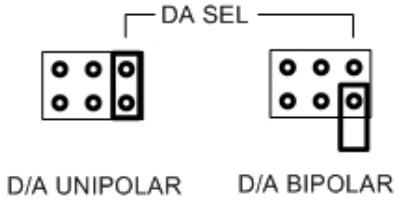
Figure 25: A/D Unipolar/Bipolar Selection




### *Analog Output Configuration Settings*

The four analog outputs can also be configured for unipolar (positive voltages only) or bipolar (both positive and negative output voltages). In unipolar mode, the outputs range between 0-10V. In bipolar mode, the outputs range between ±10V. Install the jumper for unipolar mode, as shown below. The default configuration is bipolar mode (jumper out).

Figure 26: Analog Output Configuration Selection

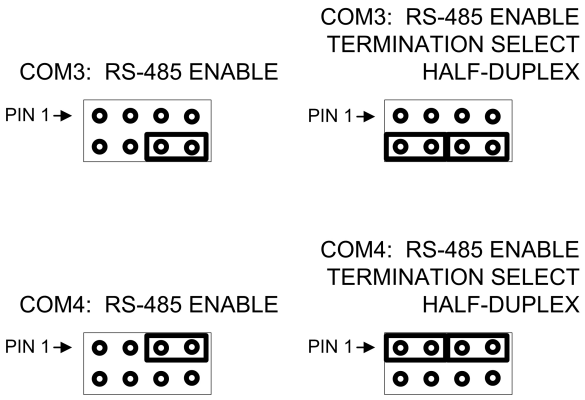



If the jumper is in, the outputs resets to the bottom of their range (zero-scale). If the jumper is out, the outputs resets to the middle of their range (mid-scale). Normally, the D/A is configured to power up to 0V. When the power is turned on, the device connected to the analog output does not see a step change in voltage. Therefore, for unipolar mode, the outputs should normally be configured for zero-scale reset, and for bipolar mode the outputs should be configured for mid-scale reset because 0V is halfway between -10V and +10V, for the ±10V range.

### *RS-485 Mode Selection (J18)*

Jumper block J18 is used to select RS-485 mode for COM3/COM4.

Figure 27: J18 Jumper Block




**Note 1. RS-485 mode needs to be set in the BIOS.**

**Note 2. Echo is enabled when RS-485 is set in half-duplex mode.**

# System Operation

## *System Resources*

The table below lists the system resources utilized by the circuits on Athena II.

| *Device* | *Default Address* | *ISA IRQ* | *ISA DMA* | *Selectable Addresses* |
|---|---|---|---|---|
| Serial Port COM1 | I/O 0x3F8 – 0x3FF | 3.4 | – | 2F8, 3E8, 2E8 |
| Serial Port COM2 | I/O 0x2F8 – 0x2FF | 3,4 | – | 3F8, 3E8, 2E8 |
| Serial Port COM3 | I/O 0x3E8 – 0x3EF | 3,4,5,6,9 | – | – |
| Serial Port COM4 | I/O 0x2E8 – 0x2EF | 3,15 | – | – |
| LPT Printer Port | I/O 0x378 – 0x37F | 5,7 | 3 | 278, 3BC |
| IDE Controller A | I/O 0x1F0 – 0x1F7 | 14 | – | – |
| A/D Circuit (when applicable) | I/O 0x280 – 0x28F | 4,5,6 | – | – |
| Watchdog Timer/Serial Port/FPGA | I/O 0x25C-0x25F | – | – | – |
| Ethernet | OS-dependent | OS-dependent | – | – |
| USB | OS-dependent | OS-dependent | – | – |
| Sound | OS-dependent | OS-dependent | – | – |
| Video | OS-dependent | OS-dependent | – | – |

**Note: In the preceding table, the selectable addresses are declared in CMOS BIOS.**

Most of these resources are configurable and, in many cases, the Operating System alters these settings. The main devices that are subject to this dynamic configuration are on-board Ethernet, sound, video, USB, and any PC/104-*Plus* cards that are in the system. These settings may also vary depending on what other devices are present in the system. For example, adding a PC/104-*Plus* card may change the on-board Ethernet resources.

The serial port settings for COM3 and COM4 are jumper-selectable (J10), whereas the settings for COM1 and COM2 are entirely software-configured in the BIOS.

## *Console Redirection to a Serial Port*

In many applications without a local display and keyboard, it may be necessary to obtain keyboard and monitor access to the CPU for configuration, file transfer, or other operations. Athena II supports this operation by enabling keyboard input and character output onto a serial port, referred to as console redirection. A serial port on another PC can be connected to the serial port on Athena II with a null modem cable, and a terminal emulation program, such as HyperTerminal, can be used to establish the connection. The terminal program must be capable of transmitting special characters including F2 (some programs or configurations trap special characters).

The default Athena II BIOS setting disables console redirection.

There are three possible configurations for console redirection:

- POST-only (default)
- Always On
- Disabled

To modify the console redirection settings,

1. Enter the BIOS
2. Select the Advanced menu
3. Select Console Redirection.
4. In Com Port Address, select Disabled to disable the function, On-board COM A for COM1, or On-board COM B for COM2 (default).

   If you select Disabled, you will not be able to enter BIOS again during power-up through the serial port.

To reenter BIOS when console redirection is disabled, you must install a video monitor or LCD and use a keyboard. Erasing the CMOS RAM returns the BIOS to its default settings. CMOS RAM may be erased by removing the jumper on the JP10 jumper block.

**Note: Before erasing CMOS RAM, write down any custom BIOS settings you have made.**

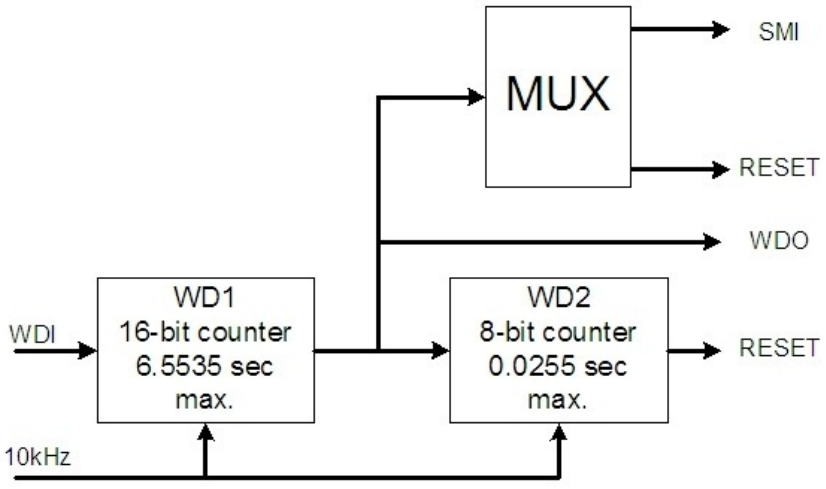
If you selected COMA or COMB, continue with the configuration, as follows.

1. For Console Type, select PC ANSI.
2. You can modify the baud rate and flow control here if desired.
3. At the bottom, for Continue C.R. after POST, select Off (default) to turn off after POST or select On to remain on always.
4. Exit the BIOS and save your settings.

## *Watchdog Timer*

Athena II contains a watchdog timer circuit consisting of two programmable timers, WD1 and WD2, cascaded together. The input to the circuit is WDI and the output is WDO. WDI may be triggered in hardware or in software. A special "early" version of WDO may be output on the WDO pin. When this signal is connected to WDI, the watchdog circuit is re-triggered automatically. The watchdog timer block diagram is shown in Figure 28.

Figure 28: Watchdog Timer Block Diagram



The duration of each timer is user-programmable. When WD1 is triggered, it begins to count down. When it reaches zero, it triggers WD2, sets WDO high, and may also generate a user-selectable combination of the following events.

- System Management interrupt (SMI)
- Hardware reset

WD2 then begins to count down. When the WD2 counter reaches zero, it unconditionally causes a hardware reset. The WD2 timer gives external circuits time to respond to the WDO event before the hardware reset occurs.

The watchdog timer circuit is programmed via I/O registers located on Page 0: Base +28-31. The Athena II watchdog timer is supported in the Diamond Systems Universal Driver software version 5.7 and later.

## *Flash Memory*

Athena II contains a 512KB, 16-bit wide flash memory chip for storage of BIOS and other system configuration data.

## *Backup Battery*

Athena II contains an integrated RTC/CMOS RAM backup battery. This battery has a capacity of 120mAH and will last over three years in power-off state.

The on-board battery is activated for the first time during initial factory configuration and test. Storage temperature of the board can affect the total battery life. Storage at 23ºC is recommended.

## *System Reset*

Athena II contains a chip to control system reset operation. Reset occurs under the following conditions.

- User causes reset with a ground contact on the *Reset* input.
- Input voltage drops below 4.75V.
- Over-current condition on output power line .

The ISA Reset signal is an active high pulse with a 200ms duration. The PCI Reset is active low, with a typical pulse width duration of 200 msec.

## *On-Board Video*

Using the the on-board VIA Mark processor, Athena II integrates all of the support needed for modern media. Refer to the VIA Technologies, Inc. documentation for the Mark processor, listed in the Additional Information section of this document.

# BIOS

Athena uses a BIOS from Phoenix Technologies modified to support the custom features of the Athena board.

(See the detailed BIOS settings in Appendix A, BIOS Settings.)

## *BIOS Settings*

To change the following BIOS settings, press F2 during system startup power on self-test (POST).

### *Serial Ports*

The address and interrupt settings for serial ports COM1 and COM2 may be modified. COM1 and COM2 address and interrupt settings are configured using the Advanced, Advanced Chipset Control, I/O Chip Device Configuration menu.

The addresses of COM3 and COM4 are fixed. The IRQ selections for COM3 and COM4 are configured using jumper block J10.

### *Parallel Port*

The parallel port is configured using the Advanced, I/O Chip Device Configuration menu. The port is set by default to ECP mode and located at address 0x378, IRQ 7 and DMA 3.

### *LCD Video Settings*

Athena provides direct digital support for LVDS-based LCD interfaces only. As such, there are two settings that affect this support during BIOS boot.

- Boot Video Device – By default, this is set to "AUTO". With the AUTO setting, the system attempts to identify an RGB monitor (via DDC). If no RGB monitor is detected, the system enables LCD support. If you choose to use the LCD display regardless of standard monitor connection (i.e., with both connected at once), set "Boot Video Device" to "Both".
- Panel Type – This setting defaults to "7". Do not alter this setting unless specifically instructed to do so. This setting affects the LCD display modes supported; mode "7" is the only setting currently supported. Not all LCD displays are supported.

### *Miscellaneous Settings*

- Memory Cache

Unless there is a specific reason to change these settings, it is best to keep these settings as-is. Certain system functions, such as USB keyboard support under BIOS menus, may be adversely affected by changes to these settings. These cache settings can make a noticeable difference for low-level BIOS calls and, as such, can severely limit performance if they are disabled.

- Advanced Chipset Control

  The following settings should be retained:

  Frame Buffer Size: 8MB

  AGP Rate: 4X

  Expansion Bus Performance: Normal

The Frame Buffer size can be increased for specific applications. Be aware, however, that an increase in this memory size will result in a decrease in overall system memory available. The AGP rate affects internal video accesses and does not affect any external bus speeds.

"Expansion Bus Performance" is an adjustment to allow an increase in ISA I/O Access speeds. For applications where ISA I/O accesses seem to be a limiting factor, this performance may be increased to "Accelerated". Be aware that increasing these timings may adversely affect system stability with external add-on PC/104 cards. This setting has no direct affect on PCI or memory speeds; it only affects ISA PC/104 devices. It is best to leave this setting at "Normal," if there are no ISA I/O performance issues.

- Advanced

  Installed O/S: (See Appendix A, BIOS Settings) Select the operating system.

  Large Disk Access Mode: (See Appendix A, BIOS Settings) Select the disk access mode.

- On-Chip Multifunction Device

  USB Device: Enabled/disable USB ports.

  Legacy Audio:

  "Legacy Audio" only affects DOS-based applications when used with the VIA-supported DOS Drivers. Enabling this setting will require system I/O, IRQ, and DMA resources. It is strongly recommended that this setting be left "Disabled."

- PCI and ISA Configuration (from the Advanced menu)

  The following setting should be retained.

  PCI IRQ Level 1-4: Auto-select for all

  PCI/PNP ISA UMB Region Exclusion: Available for all

- Power Management

  This setting is only effective under DOS. Otherwise, the OS power management settings pre-empt these settings. The only power management mode supported by the system is "Power-On Suspend." Other suspend modes are not supported and should not be used under any OS. Examples of unsupported suspend modes include, "Hibernate," under Windows, and "Suspend-to-Disk" or "Suspend-to-RAM".

- Memory Shadow

  These parameters should only be modified by advanced users. These settings can adversely affect system performance and reliability.

## *BIOS Console Redirection Settings*

For applications where the Video interfaces is not used, the textual feedback typically sent to the monitor can be redirected to a COM port. In this manner, a system can be managed and booted without using a video connection.

The BIOS allows the following configuration options for Console Redirection to a COM port.

- COM port address: Disabled (default), COM port A, or COM port B.
  - If Console Redirection is enabled here, the associated COM port (with "A" here referring to COM 1 and "B" referring to COM 2) is enabled regardless of the COM port settings elsewhere.
- "Continue CR After POST": Off (default), or On.

    - Determines whether or not the system is to wait for a carriage return over the COM port before continuing (after POST is completed and before OS starts loading).
- Baud Rate: 19.2K (default), 300, 1200, 2400, 9600, 38.4K, 57.6K, 115.2K.
- Console Connection: Direct (default) or Modem.
- Console Type: PC ANSI (default), VT100, VT100 (8-bit), PC-ANSI (7-bit), VT100+, or VT-UTF8.
- Flow Control: CTS/RTS (default), XON-XOFF, None.
- Number of video Pages to support: 1(default) to 8.

**Note: Console Redirection only works for text-based interaction. If the OS enables video and starts using direct video functions (which would be the case with a Linux X-terminal or Windows, for example), Console Redirection has no effect and video is then required.**

# System I/O

## *Ethernet*

The Ethernet chip is the National Semiconductor DP83815 MacPhyter chip, which is connected to the system via the board's internal PCI bus.

The Athena II Software CD includes Ethernet drivers for Windows XP, Windows CE, and Linux. The latest drivers can also be downloaded from National Semiconductor's website, listed in the Additional Information section of this document. (Search for "DP83815" to locate the product folder on the website).

A DOS utility program is provided for testing the chip and accessing the configuration EEPROM. Each board is factory-configured for a unique MAC address using this program. To run the program, boot the computer to DOS because the program will not run properly in a DOS window. In normal operation this program is not required.

Additional software support includes a packet driver with software to allow a full TCP/IP implementation.

## *Serial Ports*

Athena II contains four serial ports. Each port is capable of transmitting at speeds up to 115.2Kbaud. Ports COM1 and COM2 are built into the standard chipset., which are standard 16550 UARTs with 16-byte FIFOs.

Ports COM3 and COM4 are derived from an Exar 16C2850 dual UART chip and include 128-byte FIFOs. These ports may be operated at speeds to 1.5Mbaud with installation of high-speed drivers, as a custom option.

The serial ports use the following default system resources.

| *Port* | *I/O Address Range* | *IRQ* |
|---|---|---|
| COM1 | 0x3F8 - 0x3FF | 4 |
| COM2 | 0x2F8 - 0x2FF | 3 |
| COM3 | 0x3E8 - 0x3EF | 3,4,5,6,9 |
| COM4 | 0x2E8 - 0x2EF | 3,15 |

The COM1 and COM2 settings may be changed in the system BIOS. Select the *Advanced* menu, followed by *I/O Device Configuration,* to modify the base address and interrupt level.

The addresses of COM3 and COM4 are fixed. The IRQ settings for COM3 and COM4 are selected using jumper block J10. COM3 can use IRQ3, IRQ4, IRQ5, IRQ6 or IRQ9, and COM4 can use IRQ3 or IRQ15, as described in the Board Configuration section of this document.

> **Note: Once these jumper selections are made, the user must update the Serial Port IRQ settings to match these selections. The IRQ settings are NOT autodetected in the same way as the address settings.**

## *PS/2 Ports*

Athena II supports two PS/2 ports.

- Keyboard
- Mouse

The PS/2 ports are accessible using a cable assembly (DSC#C-PRZ-01) attached to connector J3. Support for these ports is independent of, and in addition to, mouse and keyboard support using the USB ports.

### *USB Ports*

Four USB 1.1 ports, USB0 through USB3, are accessible using cable assemblies attached to connector J5.

USB support is intended primarily for the following devices (although any USB-standard device should function).

- Keyboard
- Mouse
- USB Floppy Drive (This is required for Crisis Recovery of boot ROM)
- USB flash disk

The BIOS supports the USB keyboard during BIOS initialization screens and legacy emulation for DOS-based applications.

The USB ports can be used for keyboard and mouse at the same time that the PS/2 keyboard and mouse are connected.

# Notes on Operating Systems and Booting Procedures

## *Windows Operating System Installation Issues*

Windows operating systems installation should follow these steps, or some device drivers may not function correctly under Windows.

1. Enable CD-ROM support in the BIOS. Change the boot sequence in the BIOS so the system boots from CD-ROM first.

2. Insert the Windows installation CD into the CD-ROM and restart the computer.

3. Follow the manufacturer's instructions for installing Windows.

### *Driver Installation*

Drivers are provided on a CD. Please, follow the instructions included on the CD to install drivers for the different operating systems.

### *BIOS Setting for Windows*

When using any version of Windows, the Operating System selection in the BIOS setup menus should be set to Win98. Also, *Legacy Audio* must be disabled for Windows to boot properly.

### *CompactFlash Under Windows*

CompactFlash is not directly supported by Windows 98. A special driver may be available (see the vendor of your specific CompactFlash card for details). Without special drivers, Windows 98 does not recognize the CompactFlash.

CompactFlash support is built into Windows 2000 and XP.

## *DOS Operating Systems Installation Issues*

User the following sequence to install DOS operating systems: MS-DOS, FreeDOS and ROM-DOS.

1. Enable the following in BIOS:

   - Floppy Drive detection.
   - Legacy USB support.

2. Change the BIOS boot sequence so the system boots through the USB floppy drive.

3. Insert the DOS installation floppy disk into the USB floppy drive and start/restart the system.

4. Install any drivers needed.

   **Notes:**

   **1. For DOS Ethernet, set *Operating System* to *other* in the BIOS.**

   **2. DOS Sound emulation is currently not functional.**

## *CompactFlash Compatibility Issues Under DOS*

CompactFlash is incompatible with some utilities, under some versions of DOS.

- CompactFlash with ROM-DOS

The ROM-DOS FDISK utility does not work with CompactFlash drives. The ROM-DOS FORMAT and SYS do work, however. If CompactFlash already has a DOS partition, the ROM-DOS utilities can be used to FORMAT the CompactFlash and install operating system files on CompactFlash.

- CompactFlash with FreeDOS

  The FreeDOS FDISK or FORMAT utility do not work with CompactFlash. However, the FreeDOS SYS utility is functional with CompactFlash.

  - CompactFlash with MS-DOS

  The MS-DOS FDISK, FORMAT, and SYS utilities are not functional when used with CompactFlash. The MS-DOS operating system files cannot be installed on CompactFlash flash.

# Data Acquisition Circuit

Athena II contains a data acquisition subsystem consisting of A/D, D/A, digital I/O, and counter/timer features. This subsystem is equivalent to a complete add-on data acquisition module.

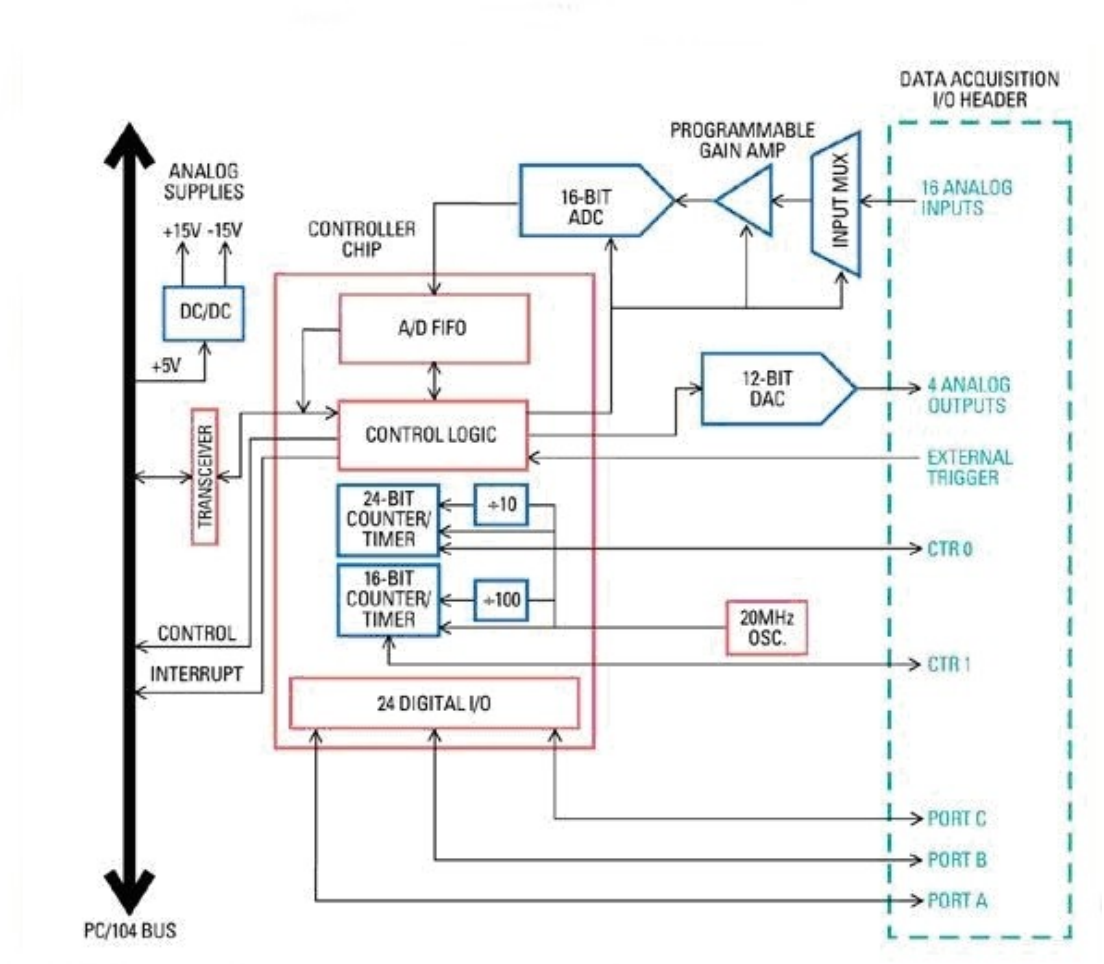
The A/D section includes a 16-bit A/D converter, 16 input channels, and a 2048-sample FIFO. Input ranges are programmable, and the maximum sampling rate is 100KHz. The D/A section includes 4 12-bit D/A channels. The digital I/O section includes 24 lines with programmable direction. The counter/timer section includes a 24-bit counter/timer to control A/D sampling rates and a 16-bit counter/timer for user applications.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store a user-selected number of samples, and the interrupt occurs when the FIFO reaches this threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate. The circuit can operate at sampling rates of up to 100KHz, with an interrupt rate of 6.6-10KHz.

The A/D circuit uses the default settings of I/O address range 280h – 28Fh (base address 280) and IRQ 5. These settings can be changed if needed. The I/O address range is changed in the BIOS, and the interrupt level is changed with jumper block J10.

Figure 29 shows a block diagram of the data acquisition circuit.

Figure 29: Athena II Data Acquisition Block Diagram



## *Data Acquisition Circuitry I/O Map*

### *Overview*

The data acquisition circuitry on Athena II occupies 16 bytes in I/O memory space. The default address range is 280h (base address) to 28Fh.

The data acquisition FPGA can be enabled/disabled in the BIOS under the Advanced menu. Scroll down to the "FPGA Mode" option and select "Enabled" or "Disabled," accordingly. If the FPGA is disabled you will not be able to interact with the data acquisition circuit. The FPGA can also be enabled or disabled programmatically through the CPLD.

### *Register Map Page Summary*

The following table summarizes the DAC register functions. The registers are paged to allow access to enhanced functions. There are three register pages and the desired page is selected using the A/D gain and scan settings register, Base+3, bits PG0-PG1, provided the board is in enhanced mode.

| ***Page 0*** | | |
|---|---|---|
| ***Base +*** | ***Write Function*** | ***Read Function*** |
| 0 | Command | A/D LSB |
| 1 | Enhanced mode control | A/D MSB |
| 2 | A/D channel | A/D channel |
| 3 | A/D gain/page select/scan settings | A/D gain and status |
| 4 | Interrupt/DMA/counter control | Interrupt/DMA/counter control |
| 5 | FIFO threshold | FIFO threshold |
| 6 | DAC LSB | FIFO depth |
| 7 | DAC MSB + channel no. | Analog operation status |
| 8 | Digital I/O port A | Digital I/O port A |
| 9 | Digital I/O port B | Digital I/O port B |
| 10 | Digital I/O port C | Digital I/O port C |
| 11 | Digital I/O control | Digital I/O control |
| 12 | Counter/timer D7-0 | Counter/timer D7-0 |
| 13 | Counter/timer D15-8 | Counter/timer D15-8 |
| 14 | Counter/timer D23-16 | Counter/timer D23-16 |
| 15 | Counter/timer control | FPGA revision code |

| ***Page 1*** | | |
|---|---|---|
| ***Base +*** | ***Write Function*** | ***Read Function*** |
| 12 | Trim DAC data/EEM data | EEM data |
| 13 | EEPROM command/Trim DAC address | EEM command address |
| 14 | Auto-CAL/Trim DAC | Trim DAC/EEM/Auto-Cal status |
| 15 | Write enable | Page 1 select read back check |

| ***Page 2*** | | |
|---|---|---|
| ***Base +*** | ***Write Function*** | ***Read Function*** |
| 12 | ADC expanded FIFO | ADC expanded FIFO |
| 13 | ADC control | ADC control |
| 14 | - | - |
| 15 | - | Page 2 select read back check |

**Note 1: Page 0, registers 0-11 are accessible when Page 1 or Page 2 are selected.**

**Note 2: In the following tables, blank bits are not used. Writes to a blank bit have no effect and reads from a blank bit return a value of zero.**

*Register Map Bit Summary*

**Page 0 Write Register Summary**

| Base + | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | STRTAD | RSTBRD | RSTDA | RSTFIFO | CLRDMA | CLRT | CLRD | CLRA |
| 1 | EM7 | EM6 | EM5 | EM4 | EM3 | EM2 | EM1 | EM0 |
| 2 | H3 | H2 | H1 | H0 | L3 | L2 | L1 | L0 |
| 3 | - | - | - | - | - | SCANEN | G1 | G0 |
| 4 | CKSEL1 | CKFRQ1 | CKFRQ0 | ADCLK | DMAEN | TINTE | DINTE | AINTE |
| 5 | - | - | FT5 | FT4 | FT3 | FT2 | FT1 | FT0 |
| 6 | DA7-DA0 | | | | | | | |
| 7 | DACH1 | DACH0 | - | - | DA11 | DA10 | DA9 | DA8 |
| 8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 9 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 10 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 11 | DIOCTR | - | - | DIRA | DIRCH | - | DIRB | DIRCL |
| 12 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 13 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 14 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| 15 | CTRNO | LATCH | GTDIS | GTEN | CTDIS | CTEN | LOAD | CLR |

**Page 0 Read Register Summary**

| Base + | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| 1 | AD15 | AD14 | AD13 | AD12 | AD11 | AD10 | AD9 | AD8 |
| 2 | H3 | H2 | H1 | H0 | L3 | L2 | L1 | L0 |
| 3 | STS | SD | WAIT | DACBSY | OVF | SCANEN | G1 | G0 |
| 4 | CKSEL1 | CKFRQ1 | CKFRQ0 | ADCLK | DMAEN | TINTE | DINTE | AINTE |
| 5 | - | - | FT5 | FT4 | FT3 | FT2 | FT1 | FT0 |
| 6 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 |
| 7 | DMAINT | TINT | DINT | AINT | ADCH3 | ADCH2 | ADCH1 | ADCH0 |
| 8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 9 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 10 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 11 | DIOCTR | - | - | DIRA | DIRCH | - | DIRB | DIRCL |
| 12 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 13 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 14 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| 15 | REV7 | REV6 | REV5 | REV4 | REV3 | REV2 | REV1 | REV0 |

**Page 1 Write Register Summary**

| Base + | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 12 | TDAD7-TDAD0 – or - EMM_CD7-EMM_CD0 | | | | | | | |
| 13 | EEM_CA7 | EEM_CA6 | EEM_CA5 | EEM_CA4 | EEM_CA3 | EEM_CA2 | EEM_CA1 | EEM_CA0 |
| 13 | - | - | - | - | - | TDAA2 | TDAA1 | TDAA0 |
| 14 | EEMST | | 0 | ADCMEN | TDAST | 0 | 0 | 0 |
| 15 | WREN7-WREN0 | | | | | | | |

**Page 1 Read Register Summary**

| Base + | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 12 | EEM_D7-EEM_D0 | | | | | | | |
| 13 | EEM_CA7-EEM_CA0 | | | | | | | |
| 14 | 0 | TDABSY | EEMBSY | ADCMEN | - | - | - | - |
| 15 | PG1ID | | | | | | | |

**Page 2 Write Register Summary**

| Base + | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 12 | - | - | - | - | - | - | - | ADCEXF |
| 13 | 0 | 0 | 0 | 0 | UNIBIDI | UNIBIOE | SEDIFDI | SEDIFOE |
| 14 | - | - | - | - | - | - | - | - |
| 15 | - | - | - | - | - | - | - | - |

**Page 2 Read Register Summary**

| Base + | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 12 | 0 | 0 | 0 | - | - | - | - | ADCEXF |
| 13 | 0 | 0 | 0 | 0 | UNIBIDI | UNIBIOE | SEDIFDI | SEDIFOE |
| 14 | - | - | - | - | - | - | - | - |
| 15 | PG2ID | | | | | | | |

## *Page 0 Register Definitions*

**Command: Base+0 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | STRTAD | RSTBRD | RSTDA | RSTFIFO | CLRDMA | CLRT | CLRD | CLRA |

STRTAD Start an A/D conversion (trigger the A/D) when in software-trigger mode AINTE = 0 (Base+4, bit 0). Once the program writes to this bit, the A/D conversion starts and the STS bit (base+3, bit 7) goes high. The program should then monitor STS and wait for it to go low (the value of Base+3 is less than 128 or 0x80). When STS goes, low the A/D data at Base+0 and Base+1 may be read.

When AINTE = 1 (Base+4, bit 0), the A/D cannot be triggered by writing to this bit. Instead, the A/D is triggered by a signal selected by ADCLK (Base+4 bit 5).

RSTBRD Reset the entire board excluding the D/A. Writing a 1 to this bit causes all on-board registers to be reset to 0. The effect on the digital I/O is that all ports are reset to input mode, and the logic state of their pins is determined by the pull-up/pull-down configuration setting selected by the user. All A/D, counter/timer, interrupt and DMA functions cease. However, the D/A values remain constant.

RSTDA Reset the four analog outputs. The analog outputs are reset to either mid-scale or zero-scale, depending on the jumper configuration selected by the user. A separate reset is provided for the D/A so that the user may reset the board if needed without affecting the circuitry connected to the analog outputs.

RSTFIFO Reset the FIFO depth to 0. This clears the FIFO, allowing additional A/D conversions to be stored in the FIFO starting at address 0.

CLRDMA Writing a 1 to this bit resets the DMA interrupt request flip flop.

CLRT Writing a 1 to this bit resets the timer interrupt request flip flop.

CLRD Writing a 1 to this bit resets the digital I/O interrupt request flip flop.

CLRA Writing a 1 to this bit resets the analog interrupt request flip flop.

- This register performs various functions. The register bits are not data bits but, instead, command triggers. Each function is initiated by writing a 1 to a particular bit. Writing a 1 to any bit in this register does not affect any other bit in this register. For example, to reset the FIFO, write the value 0x10 (16) to this register to write a 1 to bit 4. No other function of the register will be performed. Multiple actions can be performed, simultaneously, by writing a 1 to multiple bits, using a single write operation.

- The user's interrupt routine must write to the appropriate bit prior to exiting to reset the interrupt request flip flop, enabling future interrupts. Otherwise, the interrupt line remains high, indefinitely, and no additional interrupt requests are generated by the board.

**A/D LSB: Base+0 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |

AD7-AD0 A/D LSB data. The A/D data must be read LSB first, followed by MSB.

The A/D value is derived by reading two bytes from Base + 0 and Base + 1 and applying the following formula:

A/D value = (Base+0 value) + ((Base+1 value) * 256)

The value is interpreted as a two's complement, 16-bit number ranging from –32768 to +32767. This raw A/D value is converted to the corresponding input voltage and/or the engineering units represented by that voltage by applying additional application-specific formulas. Both conversions (conversion to volts and conversion to engineering units) may be combined into a single formula for efficiency.

**A/D MSB: Base+1 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | AD15 | AD14 | AD13 | AD12 | AD11 | AD10 | AD9 | AD8 |

AD15-AD8 A/D MSB data. The A/D data must be read LSB first, followed by MSB.
(Refer to the method for deriving the A/D value described in the Base+0 (Read) description, above.)

**Enhanced Mode Control: Base+1 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | EM7 | EM6 | EM5 | EM4 | EM3 | EM2 | EM1 | EM0 |

EM0-EM7 Enhanced mode control:
0xA5 = Enable enhanced mode.
0xA6 = Disable enhanced mode (default state).

**A/D Channel: Base+2 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | H3 | H2 | H1 | H0 | L3 | L2 | L1 | L0 |

H3-H0 High channel of A/D channel scan range.
Ranges from 0 to 15 in single-ended mode, 0 to 7 in differential mode.

L3-L0 Low channel of A/D channel scan range.
Ranges from 0 to 15 in single-ended mode, 0 to 7 in differential mode.

- The high channel must be greater than or equal to the low channel.
- When this register is written, the current A/D channel is set to the low channel, so that the next time an A/D conversion is triggered the low channel will be sampled.
- When this register is written, the WAIT bit (Base+3, bit 5) goes high for 10 microseconds to indicate that the analog input circuit is settling. During this time, an A/D conversion should not be performed because the data will be inaccurate.
- After writing a new gain setting (Base+3), the WAIT bit is also set, and the program must monitor the bit prior to starting an A/D conversion.
- The channel and gain registers can be written to in succession without waiting for the intervening WAIT signal. Only one WAIT period must be observed between the last triggering condition (write to Base+2 or Base+3) and the start of an A/D conversion.
- The A/D circuit is designed to automatically increment the A/D channel each time a conversion is generated. This allows the user to avoid needing to write to the A/D channel each time. The A/D channel rotates through the values between LOW and HIGH. For example, if LOW = 0 and HIGH = 3, the A/D channels progresses through the following sequence: 0, 1, 2, 3, 0, 1, 2, 3, 0, 1, ….
- Reading from this register returns the value previously written to it.

**Analog Input Gain/Page Select/Scan Settings: Base+3 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | - | - | PG1 | PG0 | - | SCANEN | G1 | G0 |

PG1-PG0 Page select (Page 0 - Page 2)

Standard Mode:
00 = Page 0
01 = Page 1
10 = Page 2

Reset and Enhanced Mode:
00 = Page 0
01 = Page 0
10 = Page 0

**Note: When the board is in standard mode, only page 0 can be accessed. The page mode can only be set when the register map is in enhanced mode.**

SCANEN Scan mode enable.

**Analog Input Gain/Page Select/Scan Settings: Base+3 (Write)**

1 = Each A/D trigger causes the board to generate an A/D conversion on each channel in the range LOW – HIGH. The range is set with the channel register in Base+2.

The STS bit (Base+3, bit 7) stays high during the entire scan.

0 = Each A/D trigger causes the board to generate a single A/D conversion on the current channel. The internal channel pointer increments to the next channel in the range LOW – HIGH or resets to LOW, if the current channel is HIGH.

The STS bit (Base+3, bit 7) stays high during the A/D conversion.

G1-G0 Analog input gain. The gain is the ratio of the voltage seen by the A/D converter and the voltage applied to the input pin. The gain setting is the same for all input channels.

- When this register is written, the WAIT bit (Read Base+3, bit 6) goes high for 10 microseconds to indicate that the analog input circuit is settling. During this time, an A/D conversion should not be performed because the data will be inaccurate. After writing a new gain setting, the program should monitor the WAIT bit prior to starting an A/D conversion.
- After writing a new channel selection (Base+2), the WAIT bit is also set, and the program must monitor it prior to starting an A/D conversion.
- The channel and gain registers can be written to in succession without waiting for the intervening WAIT signal. Only one WAIT period must be observed between the last triggering condition (write to Base+2 or Base+3) and the start of an A/D conversion.
- The following table lists the possible analog input ranges.

| ***G1*** | ***G0*** | ***Gain*** | ***Unipolar Range*** | ***Bipolar Range*** |
|---|---|---|---|---|
| 0 | 0 | 1 | Invalid | ±10V |
| 0 | 1 | 2 | 0 - 10V | ±5V |
| 1 | 0 | 4 | 0 - 5 V | ±2.5V |
| 1 | 1 | 8 | 0 - 2.5V | ±1.25V |

**Analog Input Status: Base+3 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | STS | SD | WAIT | DACBSY | OVF | SCANEN | G1 | G0 |

STS A/D status.

1 = A/D conversion or scan in progress.

0 = A/D is idle.

If SCANEN = 0, single conversion mode, STS goes high when an A/D conversion is started and stays high until the conversion is finished. If SCANEN = 1, scan mode enabled, STS stays high during the entire scan. After starting a conversion in software, the program must monitor STS and wait for the value to be 0 before reading A/D values from Base+0 and Base+1.

SD Single-ended/differential mode indicator.

1 = Single-ended

0 = Differential

WAIT A/D input circuit status.

1 = A/D circuit is settling on a new value.

0 = ok to start conversion.

**Analog Input Status: Base+3 (Read)**

WAIT goes high after the channel register (Base+2) or the gain register (Base+3) changes, and remains high for nine microseconds. The program should monitor this bit after writing to either the channel or gain register, and wait for the value to become 0 prior to starting an A/D conversion.

DACBSY DAC is busy updating indicator (approx. 30 µS)

1 = Busy

0 = Idle

Do not attempt to write to the DAC (Base+6 and Base+7) while the value of this bit is 1.

OVF FIFO Overflow bit. This bit indicates that the FIFO has overflowed, meaning that the A/D circuit has attempted to write data to a full FIFO. This condition occurs when data is written into the FIFO faster than the FIFO is read.

When overflow occurs, the FIFO discards additional data until it is reset. The OVF condition is sticky, with the bit remaining set until the FIFO is reset, allowing the application program to determine if overflow has occurred. If overflow occurs, then you must either reduce the sample rate or increase the efficiency of your interrupt routine and/or operating system.

SCANEN Scan mode readback. (See Base+3, write, above).

G1-G0 Gain. The gain is the ratio between the input voltage and the voltage seen by the A/D converter. The A/D always works with a maximum input voltage of 10V. A gain of two means the maximum input voltage at the connector pin is 5V.

0 = gain of 1

1 = gain of 2

2 = gain of 4

3 = gain of 8

(See the description for register Base+3, write, above).

**Interrupt/DMA/Counter Control: Base+4 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | CKSEL1 | CKFRQ1 | CKFRQ0 | ADCLK | DMAEN | TINTE | DINTE | AINTE |

CKSEL1 Clock source selection for counter/timer 1.
0 = Internal oscillator, frequency selected by CLKFRQ1
1 = External clock input CLK1 (DIO C pins must be set for ctr/timer signals)

CLFRQ1 Input frequency selection for counter/timer 1 when CKSEL1 = 1.
0 = 10MHz
1 = 100KHz

CKFRQ0 Input frequency selection for counter/timer 0.
0 = 10MHz
1 = 1MHz

ADCLK A/D trigger select when AINTE = 1.
0 = Internal clock output from counter/timer 0
1 = External clock input EXTTRIG

DMAEN Enable DMA operation.
1 = Enable
0 = Disable

TINTE Enable timer interrupts.
1 = Enable
0 = Disable

DINTE Enable digital I/O interrupts.
1 = Enable
0 = Disable

AINTE Enable analog input interrupts.
1 = Enable
0 = Disable

**NOTE: When AINTE = 1, the A/D cannot be triggered by writing to Base + 0.**

- Analog output interrupts are not supported on this board.
- Multiple interrupt operations may be performed, simultaneously. All interrupts are at the same interrupt level. The user's interrupt routine must monitor the status bits to know which circuit has requested service. After processing the data but before exiting, the interrupt routine must clear the appropriate interrupt request bit, using the Base+0 register.

**FIFO Threshold: Base+5 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | - | - | FT5 | FT4 | FT3 | FT2 | FT1 | FT0 |

FT0-FT5 FIFO threshold. When the number of A/D samples in the FIFO reaches this number, the board generates an interrupt and sets AINT high (Base+7, bit 4). The interrupt routine is responsible for reading the correct number of samples out of the FIFO.

The valid range is 1 to 48. A value of 48 is used, if a value greater than 48 is written to this register. A value of 1 is used, if 0 is written to this register. The interrupt rate is equal to the total sample rate divided by the FIFO threshold. Generally, for higher sampling rates a higher threshold should be used to reduce the interrupt rate. However, remember that the higher the FIFO threshold, the smaller the amount of FIFO space remaining to store data while waiting for the interrupt routine to respond. If a FIFO overflow condition occurs, lower the FIFO threshold and/or lower the A/D sampling rate.

**DAC LSB: Base+6 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | DA7-DA0 | | | | | | | |

DA7-DA0 D/A LSB data.

D/A data is an unsigned 12-bit value. This register must be written to before Base+7, because writing to Base+7 immediately updates the DAC.

**A/D Channel and FIFO Status: Base+6 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | FD7-FD0 | | | | | | | |

FD7-FD0 Current FIFO depth.

When in 48-sample FIFO mode, this value indicates the number of 16-bit A/D values currently stored in the FIFO. When in 2048-sample FIFO mode, this value represent the upper eight bits of an 11-bit value.

**DAC MSB + Channel No.: Base+7 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | DACH1 | DACH0 | - | - | DA11 | DA10 | DA9 | DA8 |

DACH0-1 D/A channel.
The values written to Base+6 and Base+7 are written to the selected channel, and that channel is immediately updated. The update takes approximately 20 microseconds because of the DAC serial interface.

DA8-DA11 D/A bits 8 to 11.
DA11 is the MSB. D/A data is an unsigned 12-bit value.

**Analog Operation Status: Base+7 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | DMAINT | TINT | DINT | AINT | ADCH3 | ADCH2 | ADCH1 | ADCH0 |

DMAINT DMA interrupt status.
1 = interrupt pending
0 = interrupt not pending

TINT Timer interrupt status.
1 = interrupt pending
0 = interrupt not pending

DINT Digital I/O interrupt status.
1 = interrupt pending
0 = interrupt not pending

AINT Analog input interrupt status.
1 = interrupt pending
0 = interrupt not pending

ADCH0-3 Current A/D channel. This is the channel sampled on the next conversion.

- When any of bits 7–4 are 1, the corresponding circuit is requesting service. The interrupt routine must poll these bits to determine which circuit needs service and then act accordingly.

**Digital I/O Port A: Base+8 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A0-A7 Port A data. The register direction is controlled by bits in the register Base+11, below.

**Digital I/O Port B: Base+9 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

B0-B7 Port B data. The register direction is controlled by bits in the register Base+11, below.

**Digital I/O Port C: Base+10 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

C0-C7 Port C data. The register direction is controlled by bits in the register Base+11, below.

**Digital I/O Control: Base+11 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | DIOCTR | - | - | DIRA | DIRCH | - | DIRB | DIRCL |

DIOCTR Selects counter I/O signals or digital I/O lines C4-C7, on pins 21-24 of J14. If DIOCTR = 0, the pin direction is as shown in the following table. If DIOCTR = 1, the pin direction is controlled by the DIRCH bit.

| ***Pin No.*** | ***DIOCTR = 1*** | ***DIOCTR = 0*** | ***Pin direction, for DIOCTR = 0*** |
|---|---|---|---|
| 21 | C4 | Gate0 | Input |
| 22 | C5 | Gate1 | Input |
| 23 | C6 | Clk1 | Input |
| 24 | C7 | Out0 | Output |

This bit resets to 1.

DIRA Port A direction.
0 = output
1 = input

DIRCH Port C, bits 7-4, direction.
0 = output
1 = input

DIRB Port B direction.
0 = output
1 = input

DIRCL Port C, bits 0-3, direction.
0 = output
1 = input

**Counter/Timer Bits 0-7: Base+12 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

D0-D7 LSB for counter 0 and counter 1.

When writing to this register, an internal load register is loaded. Upon issuing a Load command, using Base+15, the selected counter's LSB register is loaded with this value.

When reading from this register, the LSB value of the most recent Latch command is returned.

**Note: The value returned is NOT the value written to this register.**

**Counter/Timer Bits 8-15: Base+13 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

D8-D15 This register is the middle byte for counter 0 and the MSB byte for counter 1.

When writing to this register, an internal load register is loaded. Upon issuing a Load command, using Base+15, the selected counter's associated register is loaded with this value. For counter 0, the middle byte is loaded. For counter 1, the MSB byte is loaded.

When reading from this register, the associated byte of the most recent Latch command is returned.

**Note: The value returned is NOT the value written to this register.**

**Counter/Timer Bits 16-23: Base+14 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |

D16-D23 This register is used for 24-bit wide Counter 0, only.

When writing to this register, an internal load register is loaded. Upon issuing a Load command, using Base+15 for Counter 0, the counter's MSB register is loaded with this value. (When issuing a Load command for counter 1, this register is ignored).

When reading from this register, the MSB value of the most recent Latch command for counter 0 is returned.

**Note: The value returned is NOT the value written to this register.**

**Counter/Timer Control: Base+15 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | CTRNO | LATCH | GTDIS | GTEN | CTDIS | CTEN | LOAD | CLR |

CTRNO Select counter number: 0 or 1.

LATCH Latch the selected counter to read its value. T he counter must be latched before it is read. Reading from registers 12-14 returns the most recently latched value. If you are reading Counter 1 data, read only Base+12 and Base+13. Any data in Base+14 is from the previous Counter 0 access.

GTDIS Disable external gating for the selected counter.

GTEN Enable external gating for the selected counter. If enabled, the associated gate signal, GATE0 or GATE1, controls counting on the counter. If the GATE*n* signal is high, counting is enabled. If the GATE*n* signal is low, counting is disabled.

CTDIS Disable counting on the selected counter. The counter ignores input pulses.

CTEN Enable counting on the selected counter. The counter decrements with each input pulse.

LOAD Load the selected counter with the data written to Base+12 through Base+14 or Base+12 and Base+13, depending on which counter is being loaded.

CLR Clear the current counter, setting its value to 0.

This register is used to control the counter/timers. A counter is selected in bit 7 followed by a 1 written to any one of bits 6 – 0, to select the desired operation for that counter. The other bits and associated functions are not affected. Only one operation can be performed at a time.

**FPGA Revision Code: Base+15 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | REV7 | REV6 | REV5 | REV4 | REV3 | REV2 | REV1 | REV0 |

REV0-7 Revision code, read as a two-digit hexadecimal value. For example, a value of 0x20 is revision 2.0

## *Page 1 Register Definitions*

**Trim DAC data/EEM Data: Base+12 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | TDAD7-TDAD0 - or - EEM_CD7-EEM_CD0 | | | | | | | |

TDAD7-TDAD0 — TrimDAC data to set the DAC output value to at the selected address. TrimDAC data can only be written when TDABSY (base+14) is not set. TrimDAC address can be written by writing to this register or through the EEM mode, (EEM-WriteTDA_Data).
The reset value is zero.

EEM_CD7-EEM_CD0 — Data for the command data for the EEPROM. Data can only be written when EEMBSY (base+14) is cleared.

**EEM Data: Base+12 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | EEM_D7-EEM_D0 | | | | | | | |

EEM_D7-EEM_D0 — EEM data pointed to by EEPROM command address register (base+13).

**EEPROM Command/Trim DAC Address: Base+13 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | EEM_CA7 | EEM_CA6 | EEM_CA5 | EEM_CA4 | EEM_CA3 | EEM_CA2/ TDAA2 | EEM_CA1/ TDAA1 | EEM_CA0/ TDAA0 |

EEM_CA7-EEM_CA0 EEPROM command address when EEPROM write enable. Can only write data when EEMBSY (base+14) is cleared.

TDAA2-TDAA0 TrimDAC address, 8x8 bytes.

0: Q1,DAC1 ADCOFF range adjustment.
1: Q2,DAC2 ADCOFF fine adjustment.
2: Q3,DAC3 ADCFUL range adjustment.
3: Q4,DAC4 ADCFUL fine adjustment.
4: Q5,DAC5 DACOFF range adjustment.
5: Q6,DAC6 DACOFF fine adjustment.
6: Q7,DAC7 DACFUL range adjustment.
7: Q8,DAC8 DACFUL fine adjustment.

TrimDAC address can be written by writing to this register or through the EEM mode (). TrimDAC data can only be written when TDABSY (base+14) is not set.

Reset value is zero.

**EEM Command Address: Base+13 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | EEM_CA7-EEM_CA0 | | | | | | | |

EEM_CA7-EEM_CA0 EEPROM command address.

**Auto-CAL/Trim DAC: Base+14 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | EEMST | | 0 | ADCMEN | TDAST | 0 | 0 | 0 |

EEMST Sets the EEPROM read or write command. This flag is only executed when TDAST is set to zero.
0x10 = write command.
0x11 = read command.

ADCMEN Multiplexer auto-calibrate mode.
Set to enable auto-calibrate mode.

TDAST TDA start. Set to one to start the TrimDAC.
**Note: Write to this register after TrimDAC data end address ahs been written.**

**Trim DAC/EEM/Auto-CAL Status: Base+14 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | 0 | TDABSY | EEMBSY | ADCMEN | - | - | - | - |

TDABSY TrimDAC busy flag.
1 = TrimDAC registers do not accept data, address or the start command.

EEMBSY EEPROM busy flag.
1 = EEPROM busy.

ADCMEN Multiplexer auto-calibrate mode.
1 = auto-calibrate enabled.

**Write Enable: Base+15 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | WREN7-WREN0 | | | | | | | |

WREN7/0 EEPROM write enable.
Write the value 0xA5 before starting an EEPROM write command.
**Note: This register can only be written when EEMBSY (base+14) is cleared.**

**Page 1 Select Read Back Check: Base+15 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | PG1ID | | | | | | | |

PGID Register page 1 ID. This register always contains the value 0xA1.

## *Page 2 Register Definitions*

**ADC Expanded FIFO: Base+12 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | 0 | 0 | 0 | - | - | - | - | ADCEXF |

ADCEXF ADC expanded FIFO mode flag.
0 = Not in expanded FIFO mode.
1 = In expanded FIFO mode.

**Note: When in expanded FIFO mode, the FIFO threshold and FIFO depth bits represent the upper eight bits of an 11-bit value.**

**ADC Expanded FIFO: Base+12 (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | - | - | - | - | - | - | - | ADCEXF |

ADCEXF ADC expanded FIFO mode flag.
0 = Not in expanded FIFO mode.
1 = In expanded FIFO mode.

**ADC Control: Base+13 (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | 0 | 0 | 0 | 0 | UNIBIDI | UNIBIOE | SEDIFDI | SEDIFOE |

UNIBIDI Controls unipolar/bipolar mode setting. When set, this overrides the jumper setting.

UNIBIOE Output enable. When set, the UNIBIDI value is gated to the output.

SEDIFDI Controls single-ended/differential mode setting. When set, this overrides the jumper setting.

SEDIFOE Output enable. When set, the SEDIFDI value is gated to the output.

**Page 2 Select Read Back Check: Base+15 (Read)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | PG2ID | | | | | | | |

PGID Register page 2 ID. This register always contains the value 0xA2.

# Analog-to-Digital Input Ranges and Resolution

## *Overview*

Athena II uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However, the A/D converter uses two's complement notation, so the A/D value is interpreted as a signed integer, ranging from –32768 to +32767.

The smallest change in input voltage that can be detected is 1/(216), or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and is referred to as 1 LSB (1 Least Significant Bit).

The analog inputs on Athena II have three configuration options.

- Single-ended or differential mode
- Unipolar or bipolar mode
- Input range (gain)

The single-ended/differential and unipolar/bipolar modes are configured using jumper block J13, and apply to all inputs. The input range selection is done in software.

## *Input Range Selection*

You can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software, which allows it to be changed on a channel-by-channel basis. In general, you should select the highest gain (smallest input range) that allows the A/D converter to read the full range of voltages over which the input signals will vary. However, a gain that is too high causes the A/D converter to clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

## *Input Range Table*

The table below indicates the analog input range for each possible configuration. The polarity is set using jumper block J13, and the gain is set with the G1 and G0 bits in the register at Base+3. The Gain value in the table is provided for clarity. Note that the single-ended vs. differential setting has no impact on the input range or the resolution.

| *Polarity* | *G1* | *G0* | *Input Range* | *Resolution 1LSB* |
|---|---|---|---|---|
| Bipolar | 0 | 0 | ±10V | 305µV |
| Bipolar | 0 | 1 | ±5V | 153µV |
| Bipolar | 1 | 0 | ±2.5V | 76µV |
| Bipolar | 1 | 1 | ±1.25V | 38µV |
| Unipolar | 0 | 0 | Invalid | Invalid |
| Unipolar | 0 | 1 | 0 - 10V | 153µV |
| Unipolar | 1 | 0 | 0 - 5V | 76µV |
| Unipolar | 1 | 1 | 0 - 2.5V | 38µV |

# Performing an A/D Conversion

## *Introduction*

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software). Performing an A/D conversion according to the following steps. Each step is discussed in detail, below.

1. Select the input channel.

2. Select the input range.

3. Wait for analog input circuit to settle.

4. Initiate an A/D conversion.

5. Wait for the conversion to finish.

6. Read the data from the board.

7. Convert the numerical data to a meaningful value.

## *Select the Input Channel*

To select the input channel to read, write a low-channel/high-channel pair to the channel register at Base+2. The low four bits select the low channel, and the high four bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel.

For example, to set the board to channel 4 only, write 0x44 to Base+2). To set the board to read channels 0 through 15, write 0xF0 to Base+2.

When you perform an A/D conversion, the current channel automatically increments to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write 0x20 to base+2. The first conversion is on channel 0, the second will be on channel 1 and the third will be on channel 2. The channel counter wraps around to the beginning so the fourth conversion will be on channel 0, again.

If you are sampling the same channel repeatedly, set both high and low to the same value as in the first example, above. On subsequent conversions, you do not need to set the channel again.

## *Select the Input Range*

Select the input range from among the available ranges. If the range is the same as for the previous A/D conversion it does not need to be set again. Write this value to the input range register at Base+3.

For example, for ±5V range (gain of 2), write 0x01 to Base+3.

## *Wait for Analog Input Circuit to Settle*

After writing to either the channel register, Base+2, or the input range register, Base+3, allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10µS timer to assist with the wait period. Monitor the WAIT bit at Base+3, bit 5. When the bit value is 1, the circuit is actively settling on the input signal. When the value is 0, the board is ready to perform A/D conversions.

### *Perform an A/D Conversion on the Current Channel*

After the above steps are completed, start the A/D conversion by writing to Base+0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base,0x80);
```

### *Wait for the Conversion to Finish*

The A/D converter chip takes up to five microseconds to complete one A/D conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, the read will occur faster than the A/D conversion and return invalid data. Therefore, the A/D converter provides a status signal to indicate whether it is busy or idle. This bit can be read back from the status register at Base+3, bit 7. When the A/D converter is busy (performing an A/D conversion), the bit value is 1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), this bit value is 0 and the program may read the data.

The following statement is a simple example of this operation.

```
while (inp(base+3) & 0x80);  // Wait for conversion to finish before proceeding
```

The above example could hang your program if there is a hardware fault and the bit is stuck at 1. A better solution is to use a loop with a timeout, as shown below.

```
int checkstatus()    // returns 0 if ok, -1 if error
int i;
for (i = 0; i < 10000; i++)
{
    if !(inp(base+3) & 0x80) then return(0);    // conversion completed
}
return(-1);                                     // conversion did not complete
```

### *Read the Data from the Board*

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and is read back in two 8-bit bytes. The LSB must be read from the board before the MSB because the data is inserted into the board's FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, because each time a byte is read from the FIFO the internal FIFO pointer advances and that byte is no longer available. Reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value.

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

The final data are interpreted as a 16-bit signed integer in the range -32768 to +32767.

> **Note: The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula, as discussed below.**

In scan mode, the behavior is the same except when the program initiates a conversion, all channels in the programmed channel range will be sampled once and the data will be stored in the FIFO. The FIFO depth register increments by the scan size. When STS goes low, the program should read out the data for all channels.

### *Convert the numerical data to a meaningful value*

Once the A/D value is read, it needs to be converted to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards, you may need to convert the voltage to some other engineering units. For example, the voltage may come from a temperature sensor and the voltage would then need to be converted to the corresponding temperature, according to the temperature sensor's characteristics.

Since there are a large number of possible input devices, this secondary step is not included here. Only conversion to input voltage is described. However, you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas.

#### *Conversion Formula for Bipolar Input Ranges*

Input voltage = A/D value / 32768 * Full-scale input range

Example:

Given, Input range is ±5V and A/D value is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The table, below, shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage).

| *A/D Code* | *Input Voltage Symbolic Formula* | *Input Voltage for ±5V Range* |
|---|---|---|
| -32768 | $-V_{FS}$ | -5.0000V |
| -32767 | $-V_{FS}$ + 1 LSB | -4.9998V |
| ... | ... | ... |
| -1 | -1 LSB | -0.00015V |
| 0 | 0 | 0.0000V |
| 1 | +1 LSB | 0.00015V |
| ... | ... | ... |
| 32767 | $V_{FS}$ - 1 LSB | 4.9998V |

#### *Conversion Formula for Unipolar Input Ranges*

Input voltage = (A/D value + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0-5V and A/D value is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The following table illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

| *A/D Code* | *Input Voltage Symbolic Formula* | *Input Voltage for 0–5V Range* |
|---|---|---|
| -32768 | 0V | 0.0000V |
| -32767 | 1 LSB ($V_{FS}$ / 65536) | 0.000076V |
| ... | ... | ... |
| -1 | $V_{FS}$ / 2 - 1 LSB | 2.4999V |
| 0 | $V_{FS}$ / 2 | 2.5000V |
| 1 | $V_{FS}$ / 2 + 1 LSB | 2.5001V |
| ... | ... | ... |
| 32767 | $V_{FS}$ - 1 LSB | 4.9999V |

# A/D Scan, Interrupt and FIFO Operation

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

At the end of an AD conversion, the 16-bit A/D data is latched into the 8-bit FIFO in an interleaved fashion, first LSB, then MSB. A/D Data is read out of the FIFO with 2 read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in Base + 2. When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation (AINTE = 1), the FIFO will fill up with data until it reaches the threshold programmed in the FIFO threshold register, and then the interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

If the FIFO reaches its limit of 48 samples, then the next time an A/D conversion occurs the Overflow flag OVF will be set. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the FIFORST bit in Base + 1, or a hardware reset must occur.

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold should be set to 8, 16, 24, 32, 40, or 48, but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the next A/D conversion occurs. Remember that no data is available until the interrupt occurs, so if the rate is slow the delay to receive A/D data may be long. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS. Experimentation may be necessary to determine the optimum FIFO threshold for each application.

The table on the next page describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN. The given interrupt software behavior describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

The following table describes the register settings for the A/D operating modes. (LOW and HIGH channels referenced in the table are the 4-bit channel numbers in Base+2.)

| *AINTE Base+4, bit 0* | *SCANE Base+2, bit 1* | *Operation* |
|---|---|---|
| 0 | 0 | Single A/D conversions are triggered by write to B+0.<br>STS stays high during the A/D conversion.<br>No interrupt occurs.<br>The user program monitors STS (Base+3, bit 7) and reads A/D data when STS goes low. |
| 0 | 1 | A/D scans are triggered by write to B+0. All channels between LOW and HIGH are sampled.<br>STS stays high during the entire scan (multiple A/D conversions).<br>No interrupt occurs.<br>The user program monitors STS (Base+3, bit 7) and reads A/D data when STS goes low. |
| 1 | 0 | Single A/D conversions are triggered by the source selected with ADCLK (Base+4, bit 4).<br>STS stays high during the A/D conversion.<br>A/D interrupt occurs when the FIFO reaches its programmed threshold.<br>The interrupt routine reads the number of samples equal to the FIFO threshold (Base+5, bits 0-5). |
| 1 | 1 | A/D scans are triggered by the source selected with ADCLK (Base+4, bit 4).<br>STS stays high during the entire scan (multiple A/D conversions).<br>A/D interrupt occurs when the FIFO reaches its programmed threshold.<br>The interrupt routine reads the number of samples equal to the FIFO threshold (Base+5, bits 0-5). |

# Digital-to-Analog Output Ranges and Resolution

## *Description*

Athena II uses a 4-channel 12-bit D/A converter (DAC) to provide four analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is $2^{12}$ - 1, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve.

> **Note: In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from the Athena II computer hardware to an analog signal terminating at an external source.**

## *Resolution*

The resolution is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB ). The value of this LSB is calculated as follows.

1 LSB = Output voltage range / 4096

Example:

For, Output range = 0-10V,

Output voltage range = 10V – 0V = 10V

Therefore,

1 LSB = 10V / 4096 = 2.44mV

Example:

For, Output range = ±10V;

Output voltage range = 10V – (-10V) = 20V

Therefore,

1 LSB = 20V / 4096 = 4.88mV

## *Output Range Selection*

Jumper block J13 is used to select the DAC output range. The DACs can be configured for 0-10V or ±10V.

Two parameters are configured

- unipolar/bipolar mode
- power-up/reset clear mode.

In most case, for unipolar mode configure the board to reset to zero scale, and for bipolar mode configure the board for reset to mid-scale. In each case the DACs reset to 0V.

## *D/A Conversion Formulas and Tables*

The formulas below explain how to convert between D/A codes and output voltages.

### *D/A Conversion Formulas for Unipolar Output Ranges*

Output voltage = (D/A code / 4096) * Reference voltage

D/A code = (Output voltage / Reference voltage) * 4096

Example:

For,

Output range in unipolar mode = 0 – 10V,

and,

Full-scale range = 10V – 0V = 10V,

if,

Desired output voltage = 2.000V,

D/A code = 2.000V / 10V * 4096 = 819.2 => 819

**Note: the output code is always an integer.**

For the unipolar output range 0-10V, 1 LSB = 1/4096 * 10V = 2.44mV.

The following table illustrates the relationship between D/A code and output voltage for a unipolar output range (VREF = Reference voltage).

| *D/A Code* | *Output Voltage Symbolic Formula* | *Output Voltage for 0-10V Range* |
|---|---|---|
| 0 | 0V | 0.0000V |
| 1 | 1 LSB ($V_{REF}$ / 4096) | 0.0024V |
| ... | ... | ... |
| 2047 | $V_{REF}$ / 2 - 1 LSB | 4.9976V |
| 2048 | $V_{REF}$ / 2 | 5.0000V |
| 2049 | $V_{REF}$ / 2 + 1 LSB | 5.0024V |
| ... | ... | ... |
| 4095 | $V_{REF}$ - 1 LSB | 9.9976V |

*D/A Conversion Formulas for Bipolar Output Ranges*

Output voltage = ((D/A code – 2048) / 2048) * Output reference

D/A code = (Output voltage / Output reference) * 2048 + 2048

Example:

For,

Output range in bipolar mode = ±10V

and,

Full-scale range = 10V – (-10V) = 20V

if,

Desired output voltage = 2.000V

D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

For the bipolar output range ±10V, 1 LSB = 1/4096 * 20V, or 4.88mV.

The following table illustrates the relationship between D/A code and output voltage for a bipolar output range (VREF = Reference voltage).

| ***D/A Code*** | ***Output Voltage Symbolic Formula*** | ***Output Voltage for ±10V Range*** |
|---|---|---|
| 0 | $-V_{REF}$ | -10.0000V |
| 1 | $V_{REF}$ + 1 LSB | -9.9951V |
| ... | ... | ... |
| 2047 | -1 LSB | -0.0049V |
| 2048 | 0 | 0.0000V |
| 2049 | +1 LSB | 0.0049V |
| ... | ... | ... |
| 4095 | $V_{REF}$ - 1 LSB | 9.9951V |

# Generating an Analog Output

There are three steps involved in performing a D/A conversion, or generating an analog output. Each step is described in more detail, below. The descriptions use direct programming instead of driver software.

1. Compute the D/A code for the desired output voltage.

2. Write the value to the selected output channel.

3. Wait for the D/A to update.

## *Compute the D/A Code for the Desired Output Voltage*

Use the formulas in the preceding section to compute the D/A code required to generate the desired voltage.

> **Note: The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore, the maximum possible output voltage is always 1 LSB less than the full-scale reference voltage.**

## *Write the Value to the Selected Output Channel Registers*

Use the following formulas to compute the LSB and MSB values.

LSB = D/A Code & 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example:

For,

Output code = 1776

Compute,

LSB = 1776 & 255 = 240 (0xF0)

and

MSB = int(1776 / 256) = int(6.9375) = 6

The LSB is an 8-bit number in the range 0-255. The MSB is a 4-bit number in the range 0-15.

The MSB is always rounded *down*. The truncated portion is accounted for by the LSB.

Write these values to the selected channel. The LSB is written to Base+6. The MSB and channel number are written to Base+7 (MSB = bits 0-3, channel number,0-3 = bits 6-7).

```
outp(Base+6, LSB);
outp(Base+7, MSB + channel << 6);
```

### *Wait for the D/A to Update*

Writing the MSB and channel number to Base+7 starts the D/A update process for the selected channel. The update process requires approximately 30 microseconds to transmit the data serially to the D/A chip and update the D/A circuit in the chip. During this period, no attempt should be made to write to any other channel in the D/A through addresses Base+6 or Base+7.

The status bit DACBUSY (Base+3, bit 4) indicates if the D/A is busy updating (1) or idle (0). After writing to the D/A, monitor DACBUSY until it is zero before continuing with the next D/A operation.

# Analog Circuit Calibration

Calibration applies only to boards with the analog I/O circuitry.

The analog I/O circuit is calibrated during production test prior to shipment. Over time the circuit may drift slightly. If calibration is desired, internal auto-calibration can be performed using the software routines provided with the Diamond Systems driver libraries, which are included with the Athena II development kit.

Four adjustments are possible:

- A/D bipolar offset.
- A/D unipolar offset.
- A/D full-scale.
- D/A full-scale.

## *A/D Bipolar Offset*

Potentiometer R66, BPOF, is used for this adjustment. Configure the circuit for Bipolar A/D mode. Input 0V to any input channel and perform A/D conversions on that channel. The gain setting and single-ended vs. differential mode do not matter. Adjust R66 until the A/D value is 0. To eliminate the effects of noise, it is best to take a number of readings and average the values.

## *A/D Unipolar Offset*

Potentiometer R67, UNOF, is used for this adjustment. Configure the circuit for Unipolar A/D mode. The gain setting and single-ended vs. differential mode do not matter. Input 0V to any input channel and perform A/D conversions on that channel. Adjust R67 until the A/D value is 0~1. To eliminate the effects of noise, it is best to take a number of readings and average the values.

## *A/D Full-scale*

Potentiometer R74, ADFS, is used for this adjustment. Configure the circuit for Bipolar A/D mode ±10V. Input 9.9945V to any input channel and perform A/D conversions on that channel using a gain setting of 1. Single-ended vs. differential mode does not matter. Adjust R74 until the average A/D value is 32750. To eliminate the effects of noise, it is best to take a number of readings and average the values.

Any input voltage and A/D reading near the top of the range (10V) can be used for the calibration target voltage/reading. The above value is provided as an example.

## *D/A Full-scale*

Potentiometer R89, DAFS, is used for this adjustment. Configure the D/A for 0-10V output range. Write the output code of 4095 to all four D/A channels. Measure each one and adjust R89 until the average reading is as close to 9.9976V as possible.

# Digital I/O Operation

Athena II contains 24 digital I/O lines organized as three 8-bit I/O ports: Port A, Port B, and Port C. The direction of each port is programmable, and port C is further divided into two 4-bit halves, each with independent direction. The port data are accessed at registers Base+8 through Base+10, and the port direction register is located at Base+11.

| ***Base +*** | ***7*** | ***6*** | ***5*** | ***4*** | ***3*** | ***2*** | ***1*** | ***0*** |
|---|---|---|---|---|---|---|---|---|
| 8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| 9 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| 10 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| 11 | DIOCTR | - | - | DIRA | DIRCH | - | DIRB | DIRCL |

The digital I/O lines are located at pins 1 through 24 on the I/O header J14. The lines are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state.

DIRA, DIRB, DIRCH, and DIRCL control the direction of ports A, B, C4-7 and C0-3. A direction value of 0 means output and 1 means input. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

DIOCTR is used to control the function of lines C7-C4 on the I/O connector. When DIOCTR = 1, the lines are port C7-C4. When DIOCTR = 0, the lines are used for the counter/timer.

| ***Pin No.*** | ***DIOCTR = 1*** | ***DIOCTR = 0*** | ***Pin direction for DIOCTR = 0*** |
|---|---|---|---|
| 21 | C4 | Gate0 | Input |
| 22 | C5 | Gate1 | Input |
| 23 | C6 | Clk1 | Input |
| 24 | C7 | Out0 | Output |

# Counter/Timer Operation

Athena II contains two counter/timers that provide various timing functions on the board for A/D timing and user functions. These counters are controlled with registers in the on-board data acquisition controller FPGA.

## *Counter 0 – A/D Sample Control*

Counter 0 is a 24-bit, "divide-by-n" counter used for controlling A/D sampling. The counter has a clock input, a gate input, and an output. The input is a 10MHz or 1MHz clock provided on the board and selected with bit CKFRQ0 in register Base+4, bit 5. The gate is an optional signal that can be input on pin 21 of I/O header J14 when DIOCTR (Base+11, bit 7) is 1. If this signal is not used, the counter runs freely. The output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output appears on pin 24 of the I/O header when DIOCTR is 1.

The counter operates by counting down from the programmed divisor value. When the counter reaches zero, it outputs a positive-going pulse equal to one input clock period (100ns or 1µs, depending on the input clock selected by CKFRQ0). The counter then reloads to the initial load value and repeats the process, indefinitely.

The output frequency can range from 5MHz (10MHz clock, divisor = 2) to 0.06Hz (1MHz clock divided by 16,777,215, or 224-1). The output is fed into the A/D timing circuit and can be selected to trigger A/D conversions when Base+4 register bits AINTE is 1 and ADCLK is 0. Using the control register at Base+15, the counter can be loaded, cleared, enabled and disabled. The optional gate can be enabled and disabled, and the counter value can be latched for reading.

## *Counter 1 – Counting/Totalizing Functions*

Counter 1 is similar to Counter 0 except that it is a 16-bit counter. Counter 1 also has an input, a gate and an output. These signals may be user-provided on the I/O header when DIOCTR is 0, or the input may come from the on-board clock generator. When the on-board clock generator is used, the clock frequency is either 10MHz or 100KHz, as determined by control Base+4 register bit CKFRQ1.

The output is a positive-going pulse that appears on pin 26 of the I/O header. The output pulse occurs when the counter reaches zero. When the counter reaches zero, it reloads and restarts on the next clock pulse. The output stays high for the entire time the counter is at zero; i.e., from the input pulse that causes the counter to reach zero until the input pulse that causes the counter to reload.

When DIOCTR is 0, Counter 1 operates as follows.

- It counts positive edges of the signal on pin 23 on the I/O header.
- The gate is provided on pin 22. If the signal is high, the counter counts. If the signal is low, the counter holds its value and ignore input pulses. This pin has a pull-up so the counter can operate without any external gate signal.

> **NOTE: When counting external pulses, Counter 1 only updates its read register every fourth pulse. This behavior is due to the synchronous design of the counter having to contend with the asynchronous input pulses. The count register contents are correct on the fourth pulse but remain static until four additional pulses occur on the input.**

When DIOCTR is 1, Counter 1 operates as follows.

- The counter takes its input from the on-board clock generator based on the value of the Base+4 register CKFRQ1 bit. There is no gating and the counter runs continuously.

Counter 1 may be used as either a pulse generator or a totalizer/counter. In pulse generator mode, the output signal on pin 26 is of interest. In totalizer/counter mode, the counter value is of interest and may be read by first latching the value and then reading it. The width of the pulse is equal to the time period of the selected counters clock source.

## *Command Sequences*

Diamond Systems provides driver software to control the counter/timers on Athena II. The information in this section is intended as a guide for programmers writing their own code, instead of using the driver, and to give a better understanding of the counter/timer operation.

The counter control register is located at I/O address base+15.

### *Load and Enable (Run) a Counter Sequence*

1. Write the data to the counter. For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer.

   Break the load value into 3 bytes: low, middle, and high, (Two bytes for Counter 1) and write the bytes to the data registers in any sequence.

   Counter 0:

   ```
   outp(base+12,low);
   outp(base+13,middle);
   outp(base+14,high);
   ```

   Counter 1:

   ```
   outp(base+12,low);
   outp(base+13,high);
   ```

2. Load the counter.

   Counter 0:

   ```
   outp(base+15,0x02);
   ```

   Counter 1:

   ```
   outp(base+15,0x82);
   ```

3. Enable the gate if desired. The gating may be enabled or disabled at any time. When gating is disabled, the counter counts all incoming edges. When gating is enabled, if the gate is high the counter counts all incoming edges and, if the gate is low, the counter ignores incoming clock edges.

   Counter 0:

   ```
   outp(base+15,0x10);
   ```

   Counter 1:

   ```
   outp(base+15,0x90);
   ```

4. Enable the counter. A counter may be enabled or disabled at any time. If disabled, the counter ignores incoming clock edges.

   Counter 0:

   ```
   outp(base+15,0x04);
   ```

   Counter 1:

   ```
   outp(base+15,0x84);
   ```

### *Read a Counter Sequence*

1. Latch the counter.

   Counter 0:

   ```
   outp(base+15,0x40);
   ```

   Counter 1:

   ```
   outp(base+15,0xC0);
   ```

2. Read the data.

   The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

   Counter 0:

   ```
   low=inp(base+12);
   ```

   Counter 1:

   ```
   low=inp(base+12);
   ```

```
middle=inp(base+13);    high=inp(base+13);
high=inp(base+14);
```

3. Assemble the bytes into the complete counter value.

| Counter 0: | Counter 1: |
|---|---|
| `val = high * 2^16 + middle * 2^8 + low;` | `val = high * 2^8 + low;` |

### *Disabling the Counter Gate Command*

Disabling the counter gate, as shown below, causes the counter to run continuously.

| Counter 0: | Counter 1: |
|---|---|
| `outp(base+15,0x20);` | `outp(base+15,0xA0);` |

### *Clearing a Counter Sequence*

Clear a counter to restart an operation. Normally, a counter is only cleared after stopping (disabling) and reading the counter. If you clear a counter while it is enabled, it continues to count incoming pulses so the counter value may not remain at zero.

1. Stop (disable) the counter.

| Counter 0: | Counter 1: |
|---|---|
| `outp(base+15,0x08);` | `outp(base+15,0x88);` |

2. Read the data (optional).

   The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

| Counter 0: | Counter 1: |
|---|---|
| `low=inp(base+12);`<br>`middle=inp(base+13);`<br>`high=inp(base+14);` | `low=inp(base+12);`<br>`high=inp(base+13);` |

3. Clear the counter.

| Counter 0: | Counter 1: |
|---|---|
| `outp(base+15,0x01);` | `outp(base+15,0x81);` |

# Watchdog Timer Programming

Athena II contains a watchdog timer circuit consisting of one programmable timer. The input to the circuit is WDI and the output is WDO, which appear on connector J6. WDI may be triggered in hardware or in software. A special "early" version of WDO may be output on the WDO pin. When this signal is connected to WDI, the watchdog circuit is retriggered automatically.

The watchdog timer duration is user-programmable. When WDT is triggered, it begins to count down. Upon reaching zero, it generates a user-selectable combination of the following events.

- System management interrupt
- Hardware reset

The watchdog timer circuit is programmed using I/O registers located at address 0x25C. Detailed programming information is described, below. The Athena II watchdog timer is supported in the DSC Universal Driver software version 5.7 and later.

## *Watchdog Timer Register Details*

The registers in the following table are used to program the watchdog timer.

| *I/O Address* | *Write Function* | *Read Function* |
|---|---|---|
| 0x25C | WDT trigger | None, write-only |
| 0x25D | WDT, counter | None, write-only |
| 0x25E | Watchdog control | Readback |
| 0x25F | Chip select enable/disable | Readback the last bits written |

In the tables, below, a blank bit (-) indicates the bit is unused. A blank bit in the read registers reads back as 0 or 1, unknown state.

**I/O Address: 0x25C (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | - | | | WDTRIG | - | | | |

WDTRIG Writing a 1 triggers an immediate software reload of the watchdog timer.

**I/O Address: 0x25D (Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | WDT3 | WDT2 | WDT1 | WDT0 | - | | | |

WDT4-7 Writing to bits WDT4-7 loads the watchdog timer with the 4-bit counter value. Use this register to set the countdown period. Each tick is 145ms, so the period range is 145ms to 2.175 seconds (1 to 15).

**I/O Address: 0x25E (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | WDIEN | WDOEN | WDSMI | WDEDGE | - | | | |

WDIEN 0 = Disable edges on the WDI pin, retriggering watchdog timer.
1 = Enable egdes on the WDI pin retriggering watchdog timer.

WDOEN 0 = Disable edge on WDO pin when watchdog timer reaches 1.
1 = Enable edge on WDO pin when watchdog timer reaches 1.

WDSMI 0 = Disable system management interrupt signal when watchdog timer reaches 0.
1 = Enable system management interrupt signal when watchdog timer reaches 0.

WDEDGE 0 = Falling edge on WDI retriggers watchdog timer, when WDIEN = 1.
1 = Rising edge on WDI retriggers watchdog timer, when WDIEN = 1.

**I/O Address: 0x25F (Read/Write)**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name: | COM4EN | COM3EN | FPGAEN | WDEN | - | | | |

COM4EN COM4 chip select enable.
1 = Enable COM4-CS#.
0 = Disable COM4-CS#.

COM3EN COM3 chip select enable.
1 = Enable COM3-CS#.
0 = Disable COM3-CS#.

FPGAEN FPGA chip select enable.
1 = Enable FPGA-CS#.
0 = Disable FPGA-CS#.

WDEN Watchdog enable.
1 = Watchdog timer counter enable.
0 = Watchdog timer counter disable, WDO disable, WDI disable, CPURST# disable, EXTSMI# disable.

The CPLD initializes all values to zero on power up, and the BIOS enables each resource based on BIOS settings.

### *Example: Watchdog Timer With Software Trigger*

A software trigger relies on a thread of execution to constantly trigger watchdog timer A. If the thread is ever halted, timer A decrements to zero and starts timer B. Once timer B decrements to 0, the board resets.

In this example we set the watchdog timer to a countdown period of four seconds. Longer timeout periods are typically be used for a software-based watchdog timer, to accommodate varying software latencies, such as interrupt latencies and thread pre-emption, that may delay the watchdog trigger code.

Setting up the watchdog timer:

```
outp ( 0x25D, 0xF0 );   // set all 4-bits in Watchdog Timer to 1 (time setting)
outp ( 0x25E, 0x00 );   // WDIEN=0, WDOEN=0, WDSMI=0, WDEDGE=0
BYTE b = inp ( 0x25F ); // read in the register value
b |= 0x10;              // WDEN=1
outp ( 0x25F, b );      // enable Watchdog Timer
outp ( 0x25C, 0x10 );   // trigger Watchdog Timer
```

Once triggered, the timer will count down. With the timer setup and active, run the watchdog timer trigger in a continuous thread of code.

```
while (1)
{
    outp(base + 31, 0x80);  //trigger watchdog timer
    sleep(1000);            //sleep one second
}
```

If this thread is interrupted for any reason, the board resets four seconds after the last watchdog timer trigger.

### *Example: Watchdog Timer With Hardware Trigger*

A hardware trigger relies on an external pulse to constantly trigger watchdog timer A. If the external stream of pulses ever halts, timer A decrements to zero and starts timer B. Once timer B decrements to 0, the board resets.

In this example, we will make use of the T-1 feature of timer A to automatically reset itself unless a physical connection is broken. The physical connection must be made between WDO and WDI on the data acquisition header, J9.

Since software is not involved in maintaining the timer, we can set the reset period to a much smaller value. In this example, the reset pulse travels across the physical connection every 10 milliseconds.

```
outp ( 0x25D, 0xFF); // set all 4-bits in Watchdog Timer to 1 (time setting)
outp ( 0x25E, 0xF0); // set hardware to trigger the Watchdog Timer
BYTE b = inp ( 0x25F ); // read in the register value
b |= 0x10; // WDEN=1
outp ( 0x25F, b ); // enable Watchdog Timer
```

When timer A reaches 1, a rising edge flows from WDO to WDI, resetting the timer back to 100 and lowering WDO.

When the connection from WDO to WDI is broken, the rising edge never reaches WDI and system resets.

# Data Acquisition Specifications (Data Acquisition units only)

## *Analog Inputs*

- No. of inputs: 8 differential or 16 single-ended (user selectable)
- A/D resolution: 16 bits (1/65,536 of full scale)
- Input ranges,
  - Bipolar: ±10V, ±5V, ±2.5V, ±1.25V
  - Unipolar: 0-10V, 0-5V, 0-2.5V
- Input bias current: 50nA max
- Maximum input voltage: ±10V for linear operation
- Over-voltage protection: ±35V on any analog input without damage
- Nonlinearity: ±2LSB, no missing codes
- Drift: 10PPM/$^{o}$C typical
- Conversion rate: 100,000 samples per second max
- Conversion trigger: software trigger, internal pacer clock, or external TTL signal
- FIFO: 2048 samples, programmable interrupt threshold

## *Analog Outputs*

- No. of outputs: 4
- D/A resolution: 12 bits (1/4096 of full scale)
- Output ranges,
  - Unipolar: 0-10V or user-programmable
  - Bipolar: ±10V or user-programmable
- Output current: ±5mA max per channel
- Settling time: 4µS max to ±1/2 LSB
- Relative accuracy: ±1 LSB
- Nonlinearity: ±1 LSB, monotonic

## *Digital I/O*

- No. of lines: 24
- Compatibility: 3.3V and 5V logic compatible
- Input voltage: Logic 0: -0.5V min, 0.8V max; Logic 1: 2.0V min, 5.5V max
- Input current: ±1µA max
- Output voltage: Logic 0: 0.0V min, 0.4V max; Logic 1: 2.4V min, 3.3V max
- Output current: Logic 0: 12mA max; Logic 1: -8mA max
- I/O capacitance: 10pF max

## *Counter/Timers*

- A/D pacer clock: 24-bit down counter
  - Clock source: 10MHz, 1MHz or external signal
- General purpose: 16-bit down counter
  - Clock source: 10MHz, 100KHz or external signal

# FlashDisk Module

Athena II is designed to accommodate an optional solid-state FlashDisk module. This module contains 32MB to 128MB of solid-state non-volatile memory that operates like an IDE drive without requiring additional driver software support.

| *Model* | *Capacity* |
|---|---|
| FD-32-XT | 32MB |
| FD-64-XT | 64MB |
| FD-96-XT | 96MB |
| FD-128-XT | 128MB |

Figure 30: FlashDisk Module

## *Installing the FlashDisk Module*

The FlashDisk module installs directly on the IDE connector, J16, and is held down with a spacer and two screws onto a mounting hole on the board.

The FlashDisk module contains a jumper for master/slave configuration. For master mode, install the jumper over pins 1 and 2. For slave mode, install the jumper over pins 2 and 3.

## *Configuration*

To configure the CPU to work with the FlashDisk module, enter the BIOS by pressing F2 during startup. Select the Main menu, and then select *IDE Primary Master*. Enter the settings shown in the following table.

| *Setting* | *Value* |
|---|---|
| Type | User |
| Cylinders | 489 for 32MB flashdisk |
| Heads | 4 for 32MB flashdisk |
| Sectors | 32 for 32MB flashdisk |
| Multi Sector Transfer | Disable |
| LBA Mode Control | Enable |
| 32 Bit I/O | Disable |
| Transfer Mode | Fast PIO 1 |
| Ultra DMA Mode | Disable |

Exit the BIOS and save the change. The system will now boot and recognize the FlashDisk module as drive *C:*.

## *Using the FlashDisk with Another IDE Drive*

The FlashDisk occupies the board's 44-pin IDE connector and does not provide a pass-through connector. To utilize both the FlashDisk and a notebook drive, the Diamond Systems ACC-IDEEXT adapter and cables are required.

## *Power Supply*

The 44-pin cable carries power from the CPU to the adapter board and powers the FlashDisk module and any drive using a 44-pin connector, such as a notebook hard drive.

A drive utilizing a 40-pin connector, such as a CD-ROM or full-size hard drive, requires an external power source through an additional cable. The power may be provided from the CPU's power out connector, J12, or from one of the two 4-pin headers on the ACC-IDEEXT board. Athena II cable no. 698006 may be used with either power connector to bring power to the drive.

# FlashDisk Programmer Board

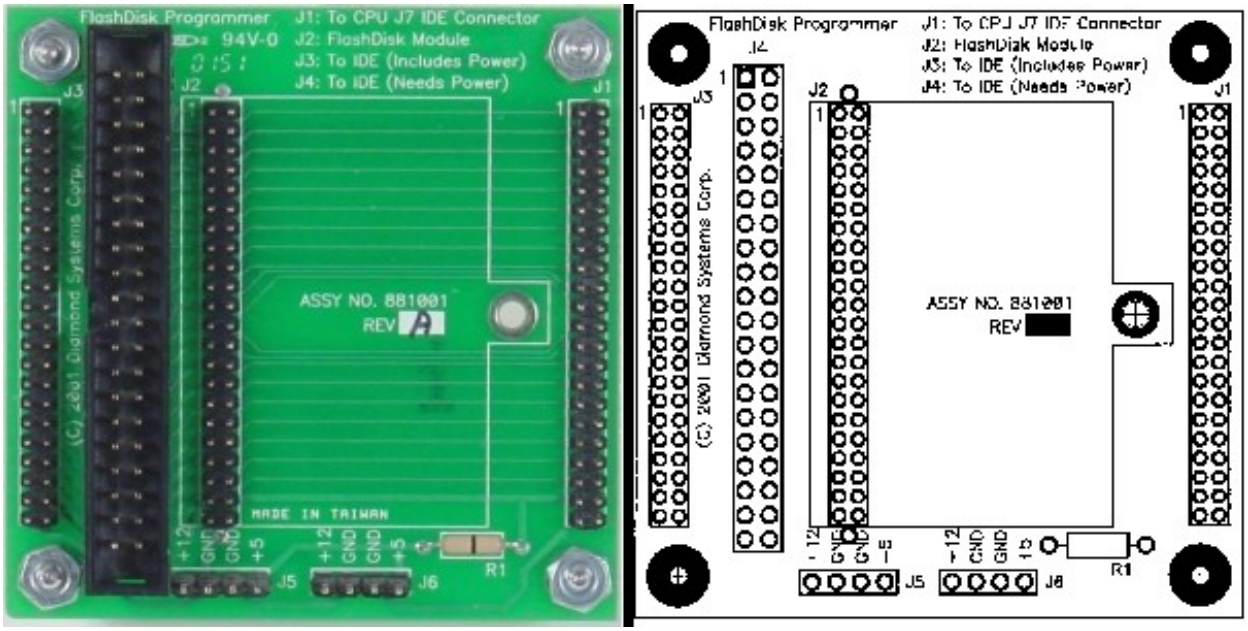
The FlashDisk Programmer Board accessory, model no. ACC-IDEEXT, may be used for several purposes. Its primary purpose is to enable the simultaneous connection of both a FlashDisk module and a standard IDE hard drive or CD-ROM drive, to allow file transfers to/from the FlashDisk. This operation is normally done at system setup. The board can also be used to enable the simultaneous connection of two drives to the CPU.

Connector J1 connects to the IDE connector on Athena II with a 44-pin ribbon cable (Diamond Systems part no. 698004). Both 40-pin .1-inch spacing, J4, and 44-pin 2mm spacing, J3, headers are provided for the external hard drive or CD-ROM drive. A dedicated connector, J2, is provided for the FlashDisk module. Any two devices may be connected simultaneously using this board with proper master/slave jumper configurations on the devices.

The FlashDisk Programmer Board comes with a 44-wire cable no. (DSC no. 698004) and a 40-wire cable no. (DSC no. C-40-18) for connection to external drives. The FlashDisk module is sold separately.

The 44-pin connector (J1, J2 and J3) and mating cable carry power, but the 40-pin connector (J4) and mating cable do not. Connectors J5 and J6 on the accessory board may be used to provide power to a 44-pin device attached to the board when the board is attached to a PC via a 40-pin cable. These headers are compatible with the floppy drive power connector on a standard PC internal power cable.

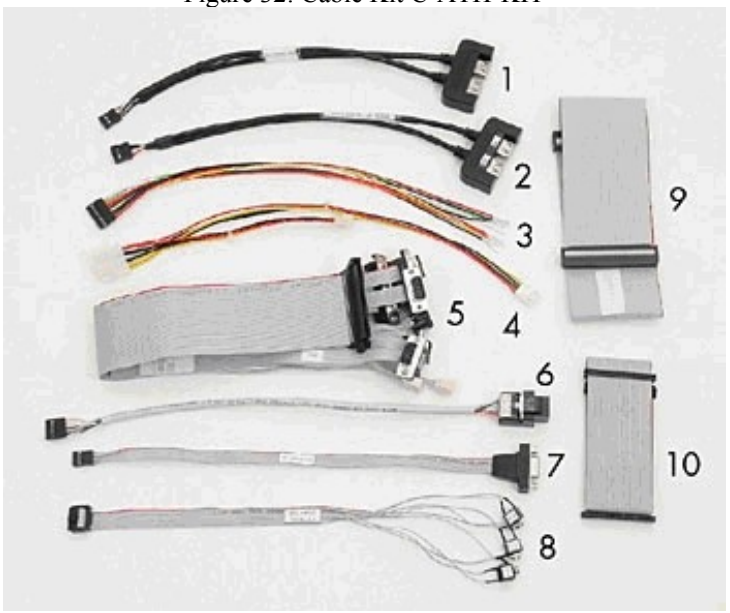
Figure 31: FlashDisk Programmer Board Layout



# I/O Cables

Diamond Systems offers cable kit C-ATH-KIT with ten cables to connect to all I/O headers on the board, shown in Figure 32. Some cables are also available separately.

Figure 32: Cable Kit C-ATH-KIT




| *Photo No.* | *Cable No.* | *Description* |
|---|---|---|
| 1 | 698032 | USB cable, ports 2 & 3 |
| 2 | 698012 | USB cable, ports 0 & 1 |
| 3 | 698009 | Power input cable |
| 4 | 698006 | Power output cable |
| 5 | C-PRZ-01 | 80-wire / 2-cable breakout cable assembly with serial, parallel, PS/2 mouse/keyboard, power, reset, speaker, & LED connectors |
| 6 | C-PRZ-02 | Ethernet cable |
| 7 | 698030 | VGA cable |
| 8 | 698031 | Audio cable |
| 9 | C-50-18 | Data acquisition, 50 conductor .1" ribbon cable |
| 10 | 698004 | IDE, 44 conductor 2mm ribbon cable |

# Quick Start Guide

This section describes the steps needed to get your Athena II board up and running, and assumes that you have also purchased the Athena Development Kit. The development kit includes all cables described in the previous section, a power supply, USB floppy drive, mounting hardware, IDE flashdisk and the flashdisk programmer board. More details about the development kit can be found at the following website:

http://www.diamondsystems.com/products/athena#dk

## *General Setup*

This section describes the initial setup procedures, which are identical regardless of which operating system or IDE configuration you are using.

1. Remove the Athena board from its packaging.

2. Install the mounting kit standoffs into the PC/104 mounting holes located at each corner of the board. This ensures that the board will not touch the surface beneath it, and helps redistribute the force when you push connectors onto the board.

3. Attach the high-density ribbon cable, C-PRZ-01, to locking connector J3. Be sure the cable is inserted snugly and the connector has locked. If you have a PS/2 mouse and keyboard, attach them to the corresponding connectors on C-PRZ-01.

4. Attach the VGA cable, 698030, to connector J25. Connect your monitor VGA cable to the DB9 socket.

5. Take the power supply out of its packaging. (Do not plug it into the wall yet). Plug the 9-pin connector into the J11 connector on the board, immediately below the PC/104 bus. Be sure the red wire, +5 VDC, goes to pin 1.

6. (Optional for Ethernet) Plug cable C-PRZ-02 into connector J4. You can use the RJ-45 socket on the C-PRZ-02 cable to patch Athena II into your network.

7. (Optional for USB Devices) You will need to connect the USB cables if you are going to use a USB floppy, keyboard or mouse. Plug USB cable 698012 into connector J5. If you need 3 or 4 USB sockets, connect cable 698032 to connector J21.

## *IDE Configuration*

Athena II has a single IDE channel that can support up to two devices simultaneously (Master and Slave). IDE devices connect through J8, which is a 44-pin, laptop IDE connector. The following are a few example setups.

1. Connect one IDE flashdisk connected directly to J8.

2. Connect one laptop IDE hard drive directly to J8 through a 44-pin ribbon cable. This cable is available in the cable kit (cable 698004).

3. Use cable 698004 to connect an IDE flashdisk programmer board to J8. You can then connect other 40-pin or 44-pin IDE compatible devices to the programmer board. Use cable 698006, attached to J12, to provide power from the Athena board to 40-pin devices. Remember, the Athena II cannot generate 12VDC. You will need to supply your own 12VDC line to the IDE device, or through the Athena II power input connector.

### *Booting into MS-DOS, FreeDOS or ROM-DOS*

This section describes how to boot into a DOS-based operating system using a bootable floppy disk.

1. Plug the USB floppy drive into one of the USB terminals of cable 698012. (Refer to step 7, above.)

2. Insert your DOS-based boot disk into the USB floppy drive.

3. Connect the power supply to the wall (to provide power to Athena II).

4. At this point the Athena II will boot and you should see the BIOS power-on self test. Press F2 to enter BIOS configuration.

5. Under the "Advanced" menu, scroll to "Legacy USB Support" and enable it. (Without enabling this option, the BIOS will not boot from a disk in the USB floppy drive).

6. Reboot the system to boot from your floppy disk.

### *Booting into Linux or Microsoft Windows*

This section describes how to setup the Athena II board in preparation for a Linux or Windows install, from an installation CD-ROM onto a laptop IDE hard drive.

1. Connect the IDE FashDisk programmer board to J8.

2. Connect a CD-ROM drive jumpered for the slave position to the IDE FlashDisk programmer board through the 40-pin cable.

3. Connect power to the CD-ROM drive using cable 698006 attached to J12. Be sure that an external 12VDC source is being suppled to J11.

4. Connect a laptop hardvdrive jumpered for master position to the second slot of the 44-pin cable.

5. Boot the Athena II by plugging the power supply into the wall.

6. Press F2 at the power-on self test to go to the BIOS configuration screen.

7. Go to the "Boot" menu and confirm that the CD-ROM drive is first boot device.

8. Insert the boot CD for your operating system into the CD-ROM drive.

9. Save the BIOS settings and reboot.

10. You should now be able to install your OS.

# Specifications

## *CPU*

- Processor: VIA Mark
- Speed: 800MHz
- Power consumption: 3.5W
- Cooling: Heat sink with fan
- Operating Temperature: -40 to +85ºC
- Chipset: VIA Mark
- System Bus: 100MHz
- SDRAM memory: 128-256MB 533MHz DDR2 soldered on-board
- Bus interface: PC/104 (ISA)
- Display type: CRT and/or 24-bit dual channel LVDS flat panel
- CRT resolution: 1600 x 1200
- Flat Panel Resolution : UXGA 1600 x 1200
- Video memory: 128MB UMA
- USB ports: (4) USB 1.1
- Serial ports: (2) RS-232 and (2) RS-232/485
- Networking: 10-/100 Base-T Ethernet
- Mass storage interfaces: (1) S-ATA, (1) IDE UDMA 100
- Keyboard/mouse: PS/2
- Audio: AC ’97, Line-in, Line-Out, Mic and amplified speaker interface

## *Data Acquisition Circuitry*

- Analog inputs: 16 single-ended, 8 differential; user selectable
- A/D resolution: 16 bits
- Bipolar ranges: ±10V, ±5V, ±2.5V, ±1.25V
- Sample rate: 250KHz max total
- Unipolar ranges: 0-10V, 0-5V, 0-2.5V, 0-1.25V
- Input bias current: 100pA max
- Protection: ±35V on any analog input without damage
- Input Impedance: 1013 ohms
- Nonlinearity: ±3LSB, no missing codes
- Conversion rate: 250,000 samples/sec. max
- On-board FIFO: 1024 samples, programmable threshold
- A/D and D/A Calibration: Automatic using on-board microcontroller and temp sensor
- Analog Outputs: 4, 12-bit resolution
- Output ranges: ±5V, ±10V, 0-5V, 0-10V
- Output current: ±5mA max per channel
- Settling time: 6µS max to 0.01%
- Relative accuracy: ±1 LSB
- Nonlinearity: ±1 LSB, monotonic
- Reset: Reset to zero-scale or mid-scale (jumper selectable)
- Waveform buffer: 1,024 samples
- Digital I/O lines: 24 programmable direction
- Input voltage: Logic 0: 0.0V min, 0.8V; maxLogic 1: 2.0V min, 5.0V max
- Input current: ±1µA max
- Output voltage: Logic 0: 0.0V min, 0.33V; maxLogic 1: 2.4V min, 5.0V max
- Output current: Logic 0: 64mA max per lineLogic 1: -15mA max per line
- A/D Pacer clock: 24-bit down counter (source: 10MHz, 1MHz or external signal)
- General purpose: 16-bit down counter (source: 10MHz, 100KHz or external signal)

### *Power Supply*

- Input Voltage: +5VDC ±5%

### *General*

- Dimensions: 4.528” x 6.496” (115mm x 165mm)
- Weight: TBD

# Additional Information

Additional information can be found at the following websites.

1. Diamond Systems Corporation: http://www.diamondsystems.com/
2. VIA Technologies, Inc.: http://www.via.com.tw/en/products/processors/corefusion/mark/index.jsp
3. National Semiconductor Corporation: http://www.national.com

# Appendix A – BIOS CMOS Option Listing

This section describes the steps for modifying the BIOS settings and describes the BIOS screens.

## *Viewing and Modifying the BIOS Settings*

During board startup, pressing function key <F2> to enter BIOS setup mode.

The main page displays the following menu options.

- Main
- Advanced
- Security
- Power
- Boot
- Exit

Select the menu option to view or modify the BIOS settings for the desired configuration area. The screens displayed for each area are described, below.

The following keyboard controls are available on any page for navigating the screen, as displayed at the bottom of each page.

| ***Key*** | ***Function*** |
|---|---|
| F1 | Help. |
| Esc | Exit current screen. |
| up-/down-arrow | Select setup item. |
| left-/right-arrow | Select menu item. |
| plus/minus symbols (+/-) | Change values. |
| Enter | Execute command. |
| F9 | Save default values. |
| F10 | Save changes and exit BIOS setup mode. |

At any time, select **Exit** to exit BIOS setup mode. Use the up/down arrow keys, followed by carriage return, to apply one of the following exit actions.

| ***Exit Action*** | ***Description*** |
|---|---|
| Exit Saving Changes | Exit BIOS setup mode saving any changes made. |
| Exit Discarding Changes | Exit BIOS setup mode discarding any changes made |
| Load Setup Default | Load default BIOS settings, without exiting BIOS setup mode. |
| Discard Changes | Discard any changes made, without exiting BIOS setup mode. |
| Save Changes | Save any changes made, without exiting BIOS setup mode. |

## *BIOS Screen Descriptions*

This section describes the screen displays for each BIOS setup area.

Where "Change Not Allowed" is indicated, it is because the configuration item is not supported by the current hardware version. The configuration item is displayed for future expansion.

### *Main*

| ***Configuration Item*** | ***Default Value or User Entry*** | ***Optional Values*** | ***Comments*** | ***Change Not Allowed*** |
|---|---|---|---|---|
| System Time | 00:00:00 | - | Hours:minutes:seconds; 24-hour format. | - |
| System Date | 00/00/00 | - | Month/day/year. | - |
| Legacy Diskette A: | DISABLED | ENABLED | - | - |
| Legacy Diskette B: | DISABLED | ENABLED | - | X |
| Primary Master | - | - | See Primary Master HDD Setup. | - |
| Primary Slave | - | - | See Primary Slave HDD Setup. | - |
| Secondary Master | - | - | See Secondary Master HDD Setup. | X |
| Secondary Slave | - | - | See Secondary Slave HDD Setup. | X |
| Memory Shadow | - | - | See Memory Shadow Setup. | - |
| Memory Cache | - | - | See Memory Cache Setup. | - |
| Quick Boot Mode | ENABLED | DISABLED | - | - |
| Floppy Check | DISABLED | ENABLED | - | X |
| System Summary Screen | DISABLED | ENABLED | - | - |
| System Memory | 640KB | - | - | X |
| Extended Memory | xxxxxxxKB | - | Determined by the BIOS. | X |

**Primary Master HDD Setup**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Device Type | AUTO | CDROM<br>User<br>ATAPI | Type of device. | - |
| Cylinders | xxxxxx | - | Number of cylinders; CHS format. | - |
| Heads | xxxxxx | - | Number of heads; CHS format. | - |
| Sectors | xxxxxx | - | Number of sectors; CHS format. | - |
| Maximum Capacity | xxxxxx | - | Always calculated by the BIOS. | X |
| Total Sector | xxxxxx | - | Total number of sectors; LBA format. Always calculated by the BIOS. | X |
| Maximum Capacity | xxxxxx | - | Maximum capacity; LBA format. Always calculated by the BIOS. | X |
| Multi-Sector Transfers | DISABLE | - | - | X |
| LBA Mode Control | DISABLE | - | - | X |
| 32 bit I/O | DISABLE | ENABLE | - | - |
| Transfer Mode | DISABLE | - | - | X |
| Ultra DMA Mode | DISABLE | - | - | X |
| Smart Monitoring | DISABLE | - | - | X |

**Primary Slave HDD Setup**

This screen is the same as the Primary Master HDD Setup screen.

**Secondary Master HDD Setup**

This screen is the same as the Primary Master HDD Setup screen.

**Secondary Slave HDD Setup**

This screen is the same as the Primary Master HDD Setup screen.

**Memory Shadow**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| System shadow | Enabled | - | - | X |
| Video shadow | Enabled | Disabled | - | - |

**Memory Cache**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Memory Cache | Enabled | Disabled | - | - |
| Cache System BIOS Area | Write-Protect | Uncached | - | - |
| Cache Video BIOS Area | Write-Protect | Uncached | - | - |
| Base 0-512KB | Write-Back | Uncached<br>Write-Through<br>Write-Protect | - | - |
| Base 512-640KB | Write-Back | Uncached<br>Write-Through<br>Write-Protect | - | - |
| Extended Memory Area | Write-Back | Uncached<br>Write-Through<br>Write-Protect | - | - |
| Cache A000-AFFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache B000-BFFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache C800-CBFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache CC00-CFFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache D000-D3FF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache D400-D7FF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache D800-DBFF | Disabled | USWC<br>Write-Through<br>Write-Protect | - | - |

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| | | Write-Back | | |
| Cache DC00-DFFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache E000-E3FF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache E400-E7FF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache E800-EBFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |
| Cache EC00-EFFF | Disabled | USWC<br>Write-Through<br>Write-Protect<br>Write-Back | - | - |

*Advanced*

**Note: Setting items on this menu to incorrect values may cause your system to malfunction.**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| PCI Configuration | - | - | See PCI Configuration. | - |
| Advanced Chipset Control | - | - | See Advanced Chipset Control. | - |
| I/O Device Configuration | - | - | See I/O Device Configuration. | - |
| PS/2 Mouse | Auto Detect | Disabled<br>Enabled | - | - |
| LAN | Disabled | Enabled | - | - |
| FPGA Mode | Disabled | Enabled | - | - |
| Boot Video Device | Auto | Both | - | - |
| LCD Panel Type | 7 | 0-F | - | - |
| Local Bus IDE Adapter | Both | Disabled<br>Primary<br>Secondary | - | - |
| Legacy USB Support | Enabled | Disabled | - | - |
| On-chip Multi-function Device | - | - | See On-chip Multi-function Device. | - |
| Large Disk Access Mode | DOS | Other | - | - |
| Installed O/S | Win98 | Other<br>Win95<br>WinME<br>Win2000 | - | - |
| Reset Configuration Data | No | Yes | - | - |
| Console Redirection | - | - | See Console Redirection. | - |
| Hardware Monitor | - | - | See Hardware Monitor. | - |

**PCI Configuration**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| PCI/PNP ISA UMB Region Exclusion | - | - | See PCI/PNP ISA UMB Region Exclusion. | - |
| PCI/PNP ISA IRQ Resource Exclusion | - | - | See PCI/PNP ISA IRQ Resource Exclusion. | - |
| PCI/PNP ISA DMA Resource Exclusion | - | - | See PCI/PNP ISA DMA Resource Exclusion. | - |
| PCI IRQ Line 1 | Disabled | Auto Select 3,4,5,6,7,8,9,10, 11,12,13,14,15 | - | - |
| PCI IRQ Line 2 | Disabled | Auto Select 3,4,5,6,7,8,9,10, 11,12,13,14,15 | - | - |
| PCI IRQ Line 3 | Disabled | Auto Select 3,4,5,6,7,8,9,10, 11,12,13,14,15 | - | - |
| PCI IRQ Line 4 | Disabled | Auto Select 3,4,5,6,7,8,9,10, 11,12,13,14,15 | - | - |

**PCI/PNP ISA UMB Region Exclusion**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| C800-CBFF | Available | Reserved | - | - |
| CC00-CFFF | Available | Reserved | - | - |
| D000-D3FF | Available | Reserved | - | - |
| D400-D7FF | Available | Reserved | - | - |
| D800-DBFF | Available | Reserved | - | - |
| DC00-DFFF | Available | Reserved | - | - |

**PCI/PNP ISA IRQ Resource Exclusion**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| IRQ3 | Available | Reserved | - | - |
| IRQ4 | Available | Reserved | - | - |
| IRQ5 | Available | Reserved | - | - |
| IRQ7 | Available | Reserved | - | - |
| IRQ8 | Available | Reserved | - | - |
| IRQ10 | Available | Reserved | - | - |
| IRQ11 | Available | Reserved | - | - |
| IRQ15 | Available | Reserved | - | - |

**PCI/PNP ISA DMA Resource Exclusion**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| DMA0 | Available | Reserved | - | - |
| DMA1 | Available | Reserved | - | - |
| DMA2 | Available | Reserved | - | - |
| DMA3 | Available | Reserved | - | - |
| DMA4 | Available | Reserved | - | - |
| DMA5 | Available | Reserved | - | - |
| DMA6 | Available | Reserved | - | - |
| DMA7 | Available | Reserved | - | - |

**Advanced Chipset Control**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| PCI Delayed Transaction | Enabled | Disabled | - | - |
| Aperture Size | 64M | 2M, 4M, 8M, 16M, 32M, 128M, 256M | - | - |
| Frame Buffer Size | 8MB | None<br>2MB, 4MB, 16MB, 32MB | - | - |
| AGP Rate | 4X | 1X<br>2X | - | - |
| Expansion Bus Performance | Normal | Accelerated<br>Turbo | - | - |

**I/O Device Configuration**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Serial Port 1 | Enabled | Auto<br>Disabled | - | - |
| Base I/O Address | 3F8 | 2F8, 3E8, 2E8 | - | - |
| Interrupt | IRQ4 | IRQ3 | - | - |
| Mode | Normal | IrDA<br>ASK_IR | - | - |
| Serial Port 2 | Enabled | Auto<br>Disabled | - | - |
| Base I/O Address | 2F8 | 3F8, 3E8, 2E8 | - | - |
| Interrupt | IRQ3 | IRQ4 | - | - |
| Mode | Normal | IrDA<br>ASK_IR | - | - |
| Serial Port 3 | Enabled | Disabled | - | - |
| Base I/O Address | 3E8 | - | - | X |
| Interrupt | IRQ9 | IRQ3, IRQ4, IRQ5, IRQ6 | - | - |
| Mode | RS232 | RS485 | - | - |
| Serial Port 4 | Enabled | Disabled | - | - |
| Base I/O Address | 2E8 | - | - | X |
| Interrupt | IRQ15 | IRQ3 | - | - |
| Mode | RS232 | RS485 | - | - |

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Parallel Port | Enabled | Auto<br>Disabled | - | - |
| Mode | ECP | EPP<br>Uni-directional | - | - |
| Base I/O Address | 378 | 278, 3BC | - | - |
| Interrupt | IRQ7 | IRQ5 | - | - |
| DMA Channel | DMA3 | DMA1 | - | - |
| Data Acquisition IRQ | IRQ5 | Disabled<br>IRQ4, IRQ6 | - | - |

**On-chip Multi-function Device**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| On-Chip USB 2 Device | Enabled | Disabled | USB ports 2 and 3. | - |
| Onboard Audio | Enabled | Disabled | - | - |
| Legacy Audio | Disabled | Enabled | - | - |
| Sound Blaster | Disabled | Enabled | - | - |
| MPU-401 | Disabled | Enabled | - | - |
| Joystick | Disabled | Enabled | - | - |

**Console Redirection**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Continue C.R. after POST | Off | On | - | - |
| Baud Rate | 19.2Kbps | 300, 1200, 2400, 9600, 38.4k, 57.6k, 115.2k (bps) | - | - |
| Console Connection | Direct | Modem | - | - |
| Console Type | PC ANSI | VT100, VT100 8bit, Pc-ANSI 7bit, VT100+, VT-UTF8 | - | - |
| Flow Control | None | XON-XOFF CTS-RTS | - | - |
| COM Port Address | Disabled | COM PORT 1 COM PORT 2 | - | - |
| # of Video Pages to Support | 1 | 2-8 | - | |

**Hardware Monitor**

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Vcore | xx.xx V | - | Set by CPU. | X |
| V(2.5V) | xx.xx V | - | Set by CPU. | X |
| V(3.3V) | xx.xx V | - | Set by CPU. | X |
| CPUTEMP1 | - | - | Set by CPU. | X |
| CPU FAN SPEED | - | - | (RPM) Set by CPU. | X |

## *Security*

| *Configuration Item* | *Default Value or User Entry* | *Optional Values* | *Comments* | *Change Not Allowed* |
|---|---|---|---|---|
| Supervisor Password Is | - | - | Field is clear. | X |
| User Password Is | - | - | Field is clear. | X |
| Set Supervisor Password | ***...*** | - | Enter password. | - |
| Set User Password | ***...*** | - | Enter password. | - |

*Power*

| ***Configuration Item*** | ***Default Value or User Entry*** | ***Optional Values*** | ***Comments*** | ***Change Not Allowed*** |
|---|---|---|---|---|
| Power Savings | Disabled | Customized<br>Max Power Savings | - | - |
| Idle Mode | Off | On | - | - |
| Standby Timeout | Off | 1, 2, 4, 6, 8, 12, 16 minutes | - | - |
| Auto Suspend Timeout | Off | 5, 10, 15, 20, 30, 40, 60 minutes | - | - |
| Hard Disk Timeout | Disabled | 10, 15, 30, 45 sec.<br>1, 2, 4, 6, 8, 10, 15 min. | - | - |
| Video Timeout | Disabled | 10, 15, 30, 45 sec.<br>1, 2, 4, 6, 8, 10, 15 min. | - | - |
| Resume on LAN | On | Off | Only active when LAN is enabled. | - |
| Resume on Time | Off | On | - | - |
| Resume Time | 00:00:00 | - | - | - |

*Boot*

| ***Configuration Item*** | ***Default Value or User Entry*** | ***Optional Values*** | ***Comments*** | ***Change Not Allowed*** |
|---|---|---|---|---|
| Power Savings | Disabled | Customized<br>Max Power Savings | - | - |
| Boot Sequence | - | Hard Drive<br>CD ROM<br>USB HDD/Floppy Disk<br>Removable Device | The order is selectable using the up/down arrow keys. | - |

# Technical Support

For technical support, please email support@diamondsystems.com or contact Diamond Systems Corporation technical support at 1-650-810-2500.